

Nucleo144 H7 SMPS with STLINK V3

MB1363

H755ZIQ

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U_MB1363_Top
MB1363_Top.SchDoc

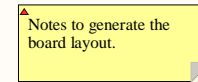


Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.



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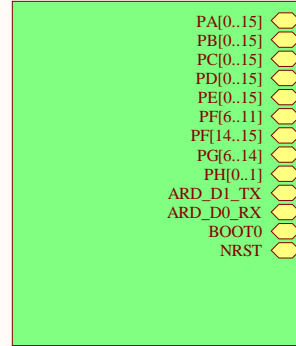
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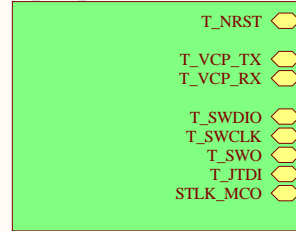
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Project: Nucleo144 H7 SMPS with STLINK V3	
Variant: H755ZIQ	
Revision: D-01	Reference: MB1363
Size: A4	Date: 09-OCT-19
Sheet: 1 of 9	



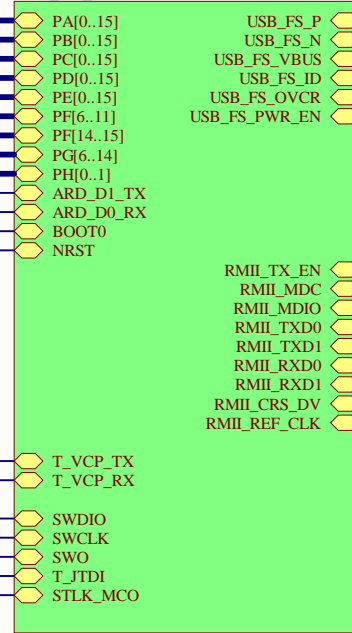
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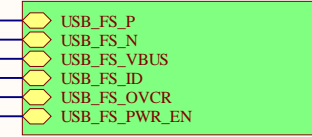
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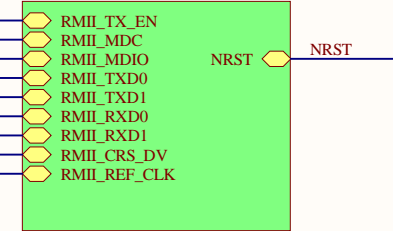
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MCU_144_IOs.SchDoc



U_USB
USB.SchDoc



U_Ethernet
Ethernet.SchDoc



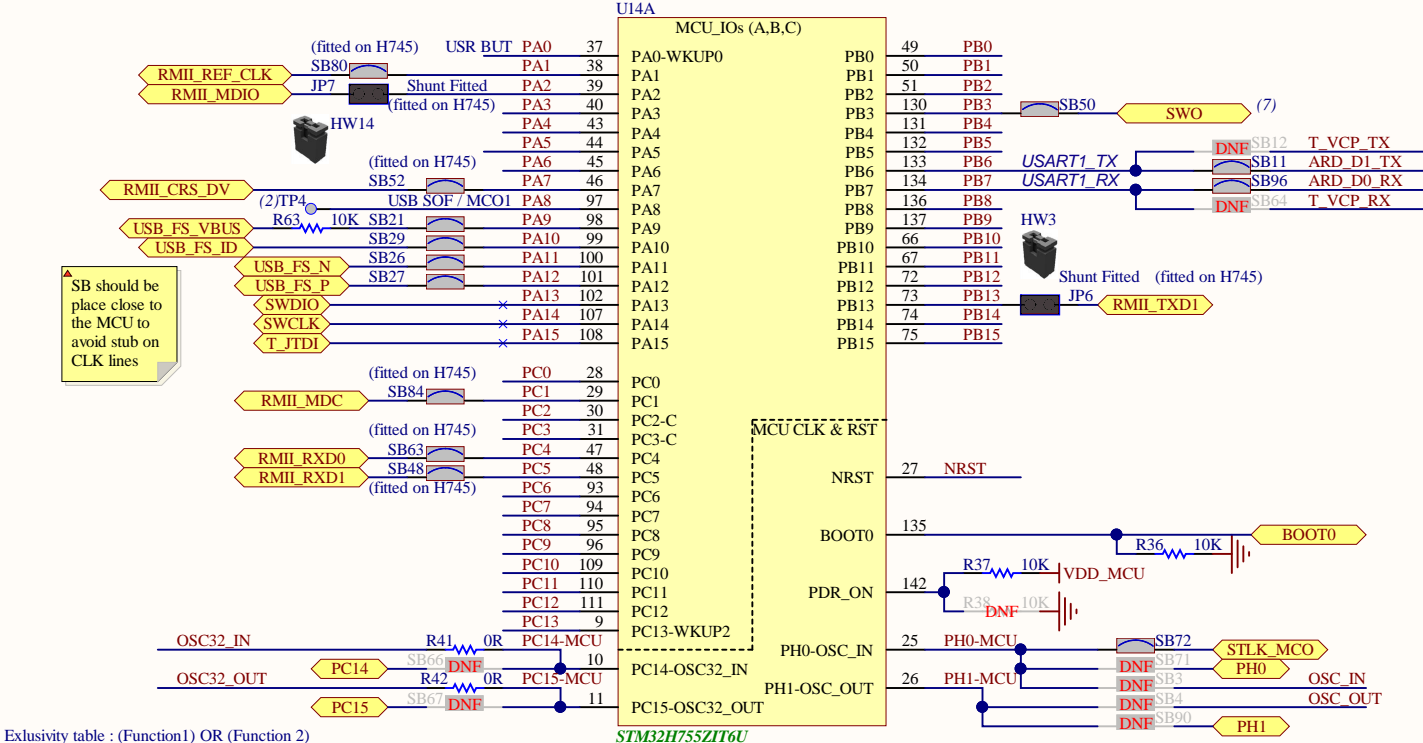
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U_Power_Board
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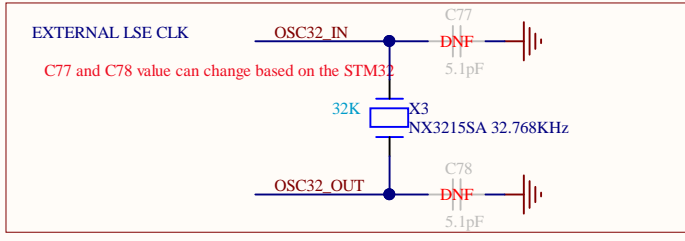
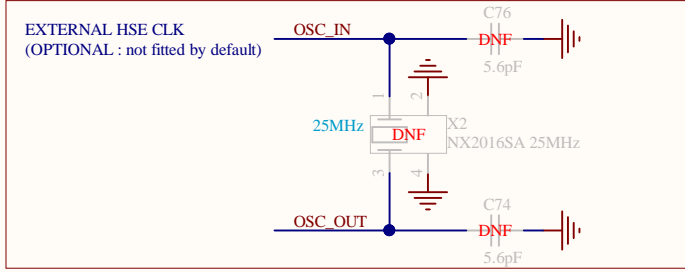
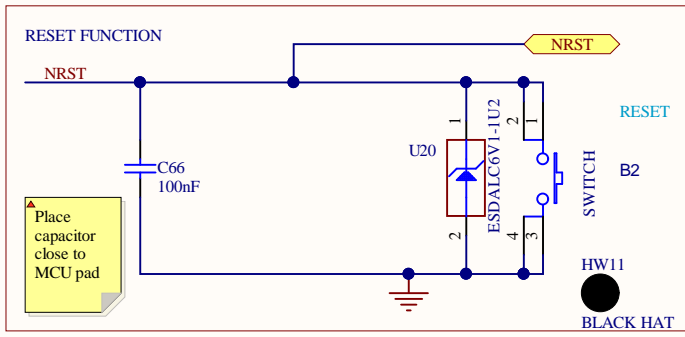
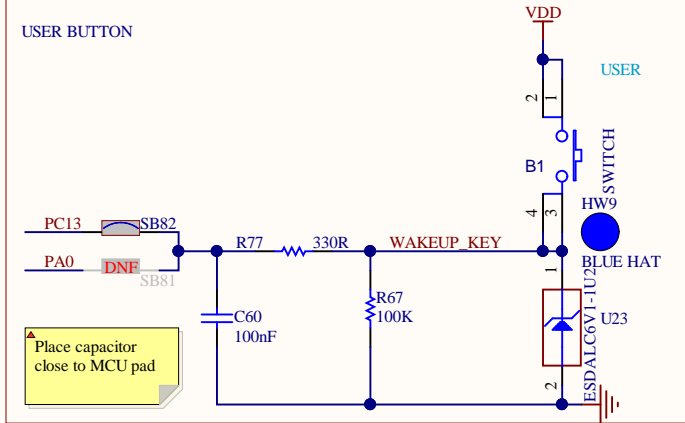
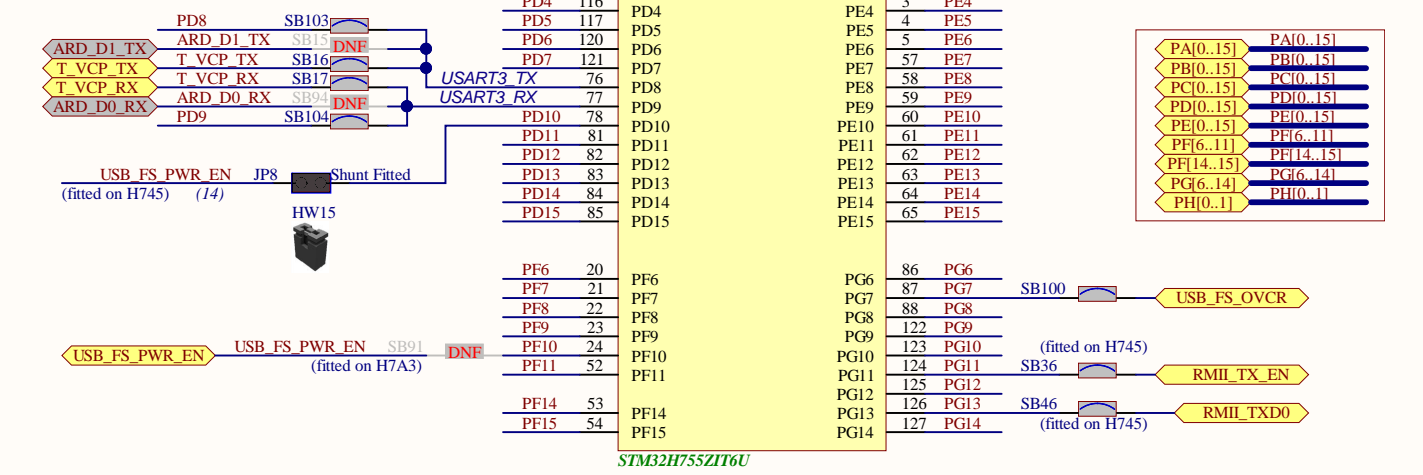


MCU IO CLK and RST

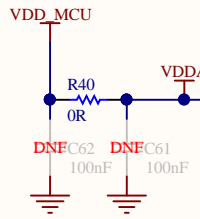
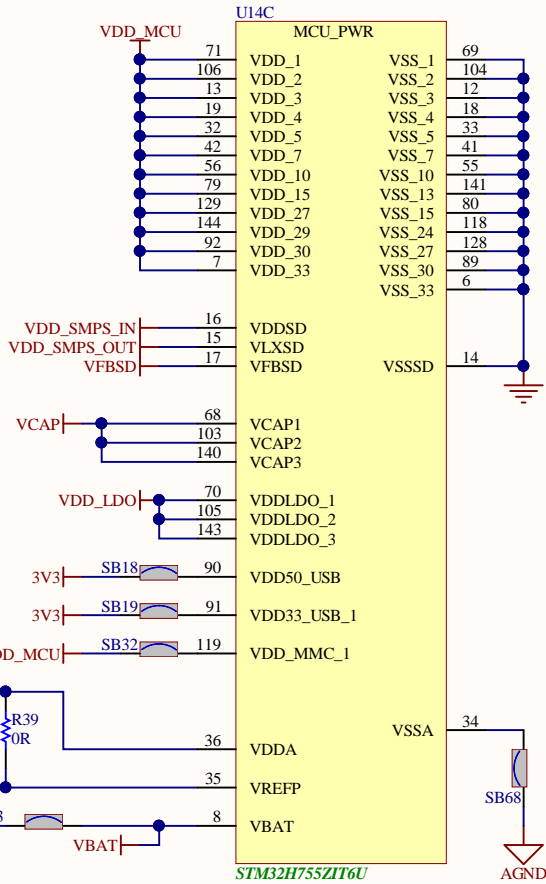
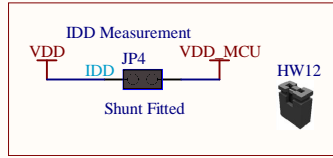


Exclusivity table : (Function1) OR (Function 2)

I/O	ARDUINO / ZIO	OTHER
(2)	PA8	D6
(5)	PA2	A8
(6)	PB13	D18
(7)	PB3	D23
(14)	PD10	D64
(15)	PB14	D65



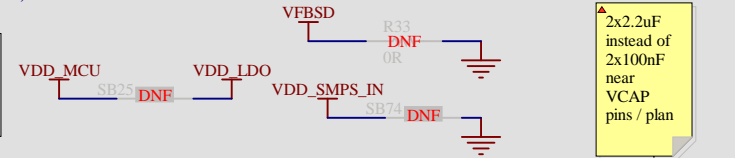
MCU PWR SUPPLIES



SMPS MCU Supply Config

Supply Config 1 : LDO only (SMPS OFF, LDO ON)

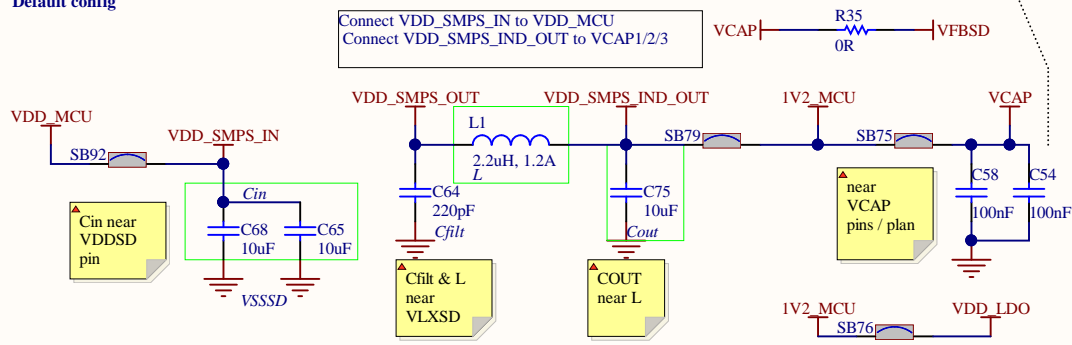
Disconnect 3V3_SMPS_IN from 3V3_MCU
Connect 3V3_SMPS_IN to GND
Connect VDD_SMPS_IND_OUT to GND
Connect VDD_LDO to 3V3_MCU
2 x 2.2uF near VCAP pins/pins



Supply Config 2 : Internal SMPS only (SMPS ON, LDO OFF)

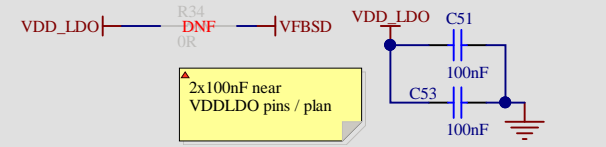
Default config

Connect VDD_SMPS_IN to VDD_MCU
Connect VDD_SMPS_IND_OUT to VCAP1/2/3



Supply Config 3 : SMPS & LDO cascaded (SMPS & LDO ON)

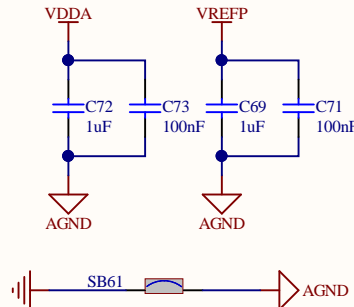
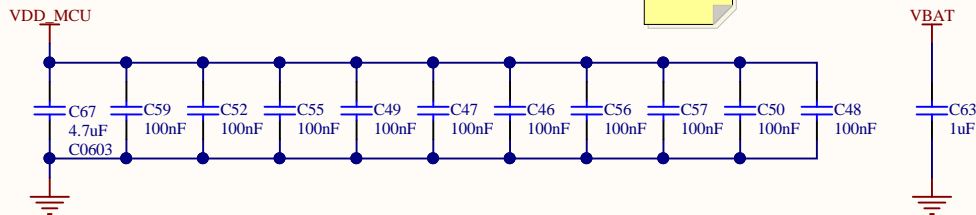
Compared to config 2 :
Disconnect VDD_SMPS_IND_OUT from VCAP
Connect VDD_SMPS_IND_OUT to VDD_LDO
Add 2x100nF near VDDLDO pins/pins
Add 2x2.2uF near VCAP pins/plans (see config 1)



Supply Config 5 : external SMPS

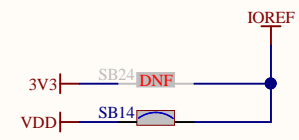
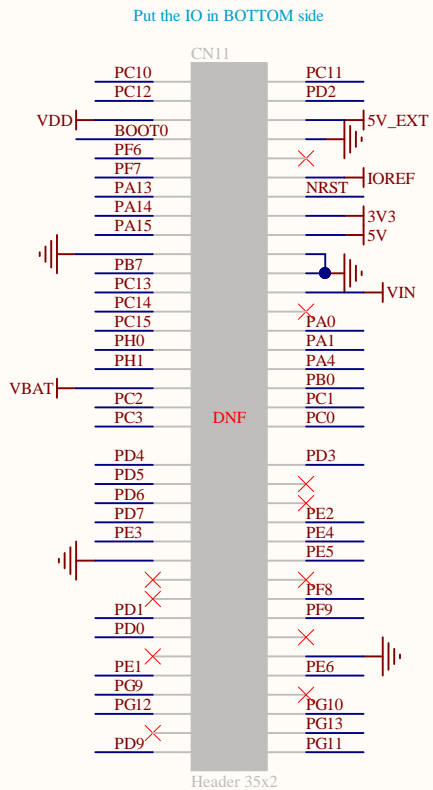
Disconnect 1V2_MCU from VDD_SMPS_IND_OUT
Connect 1V2_MCU to 1V2_VOUTCORE (Connectors page)

MCU DECAPS Ceramic capacitor (Low ESR, ESR<1ohm)

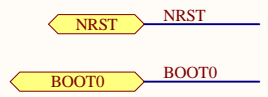


EXTENSION CONNECTORS, MCU INTERFACES

MORPHO CONNECTOR LEFT SIDE



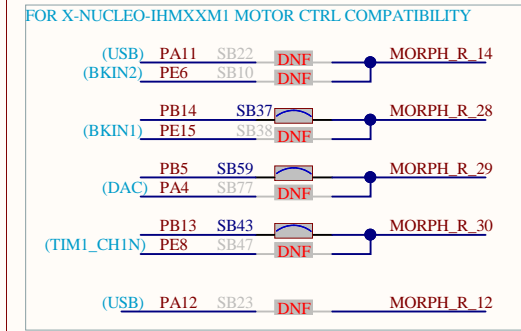
- PA[0..15] PAI0..15
- PB[0..15] PBI0..15
- PC[0..15] PCI0..15
- PD[0..15] PDI0..15
- PE[0..15] PEI0..15
- PF[6..11] PFI6..11
- PF[14..15] PFI14..15
- PG[6..14] PGI6..14
- PH[0..1] PHI0..1



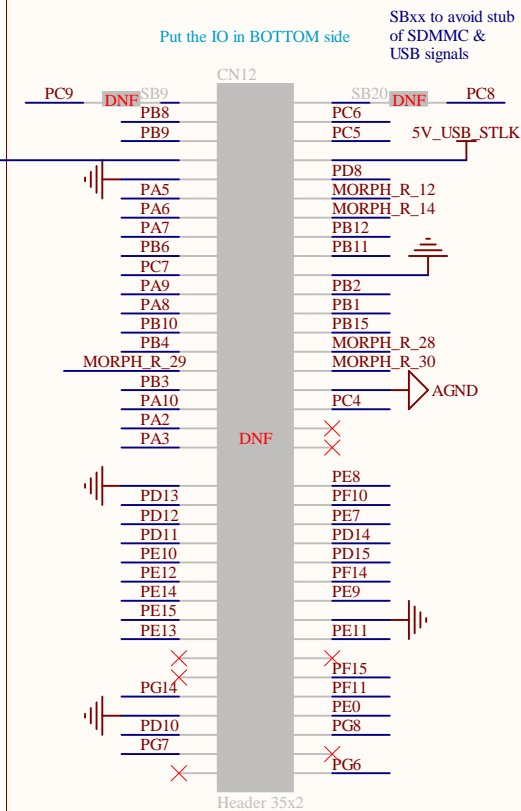
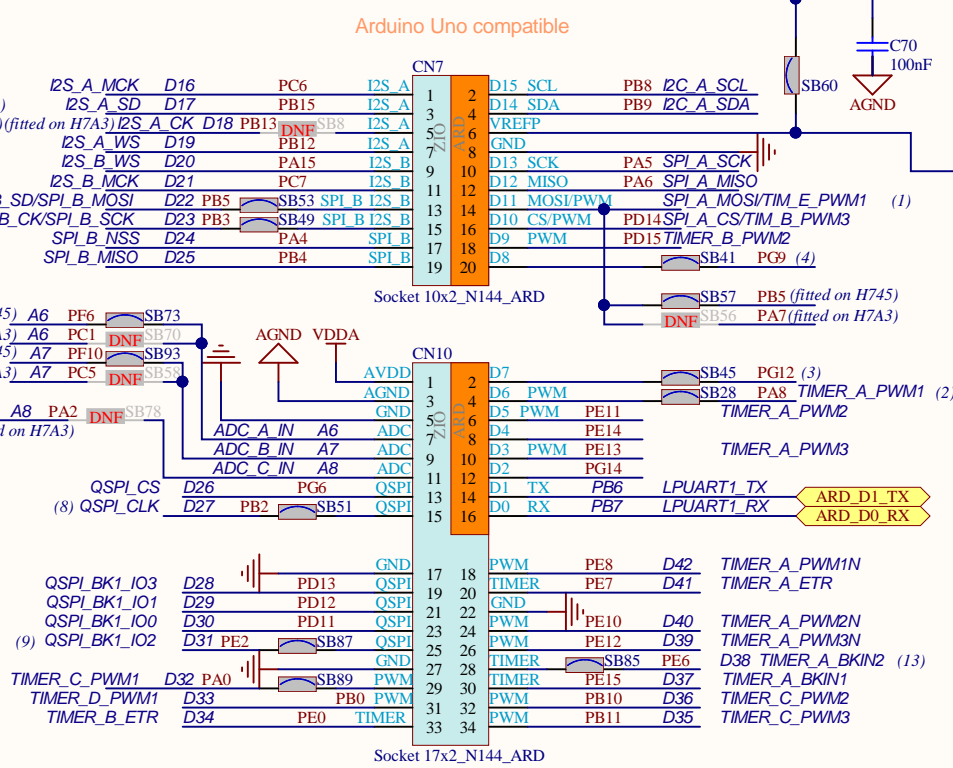
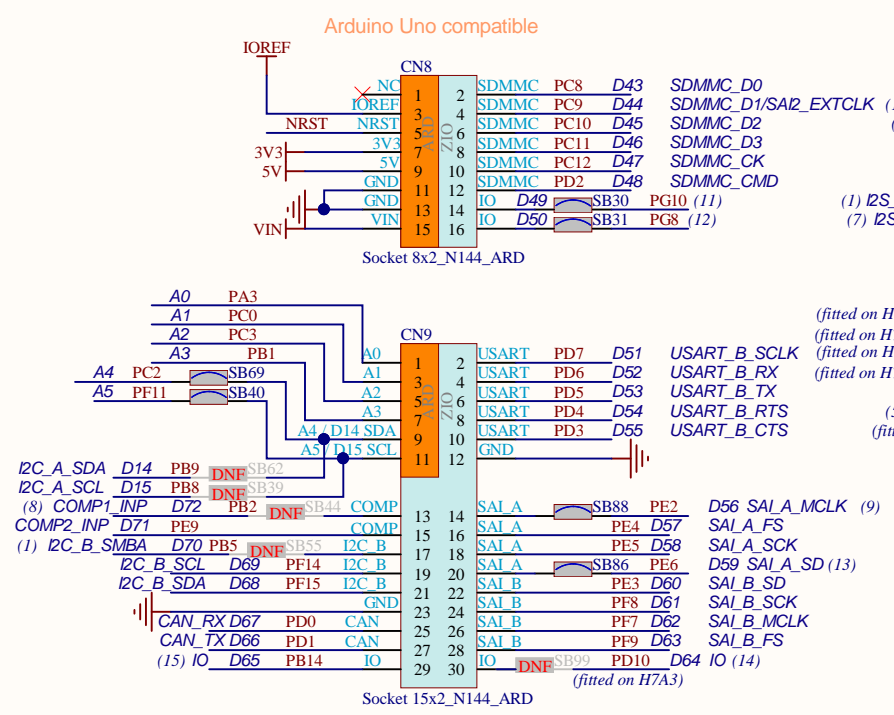
Exclusivity table : (Function1) OR (Function 2)

I/O	ARDUINO / ZIO	OTHER
(1) PB5	D11 / D22 / D70	
(2) PA8	D6	USB_SOF / MCO1
(3) PG12	D7	SMPS_PG
(4) PG9	D8	SMPS_EN
(5) PA2	A8	RMIL_MDIO (H745ZI / H755ZI)
(6) PB13	D18	RMIL_TXD1 (H745ZI / H755ZI)
(7) PB3	D23	SWO
(8) PB2	D27 / D72	
(9) PE2	D31 / D56	
(10) PC9	D44	
(11) PG10	D49	SMPS_SW
(12) PG8	D50	SMPS_V1
(13) PE6	D59 / D38	
(14) PD10	D64	USB_FS_PWR_EN (H745ZI / H755ZI)
(15) PB14	D65	LED_RED

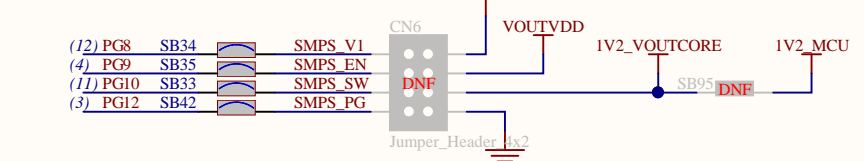
MORPHO CONNECTOR RIGHT SIDE



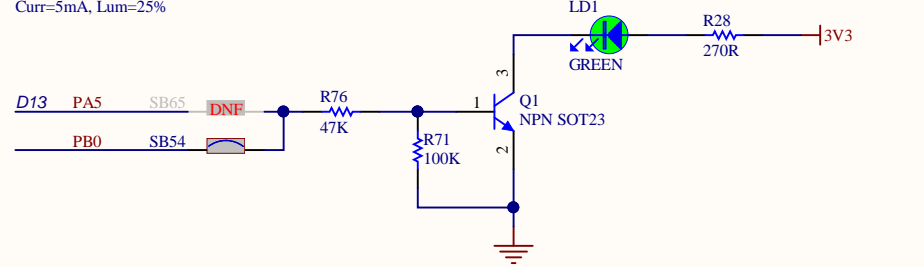
ZIO CONNECTOR ARDUINO UNO COMPATIBLE



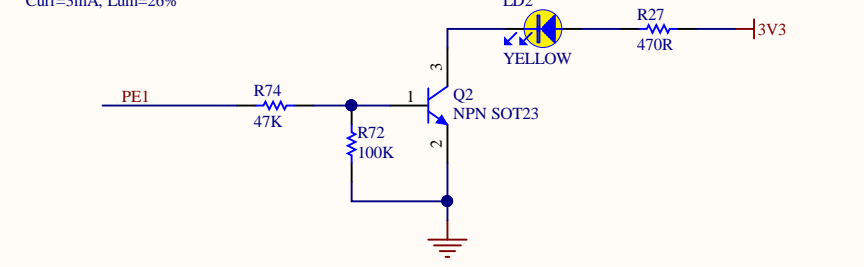
EXTERNAL SMPS SELECTION



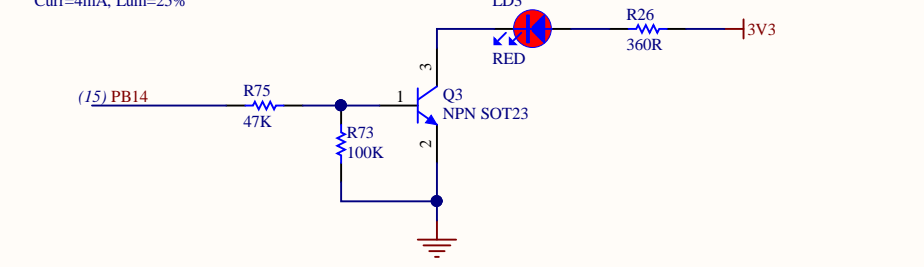
USER LED 1 : ARD_D13_LED



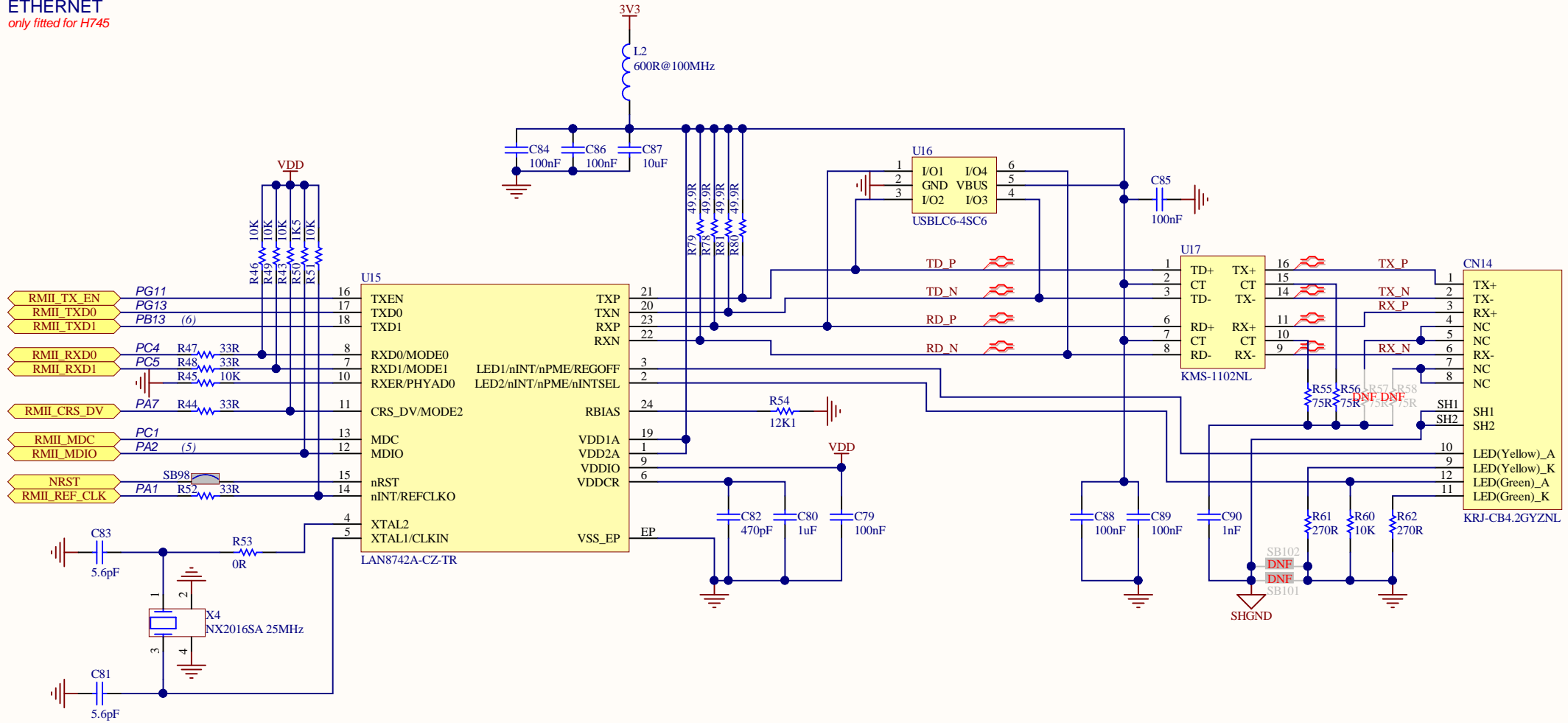
USER LED 2



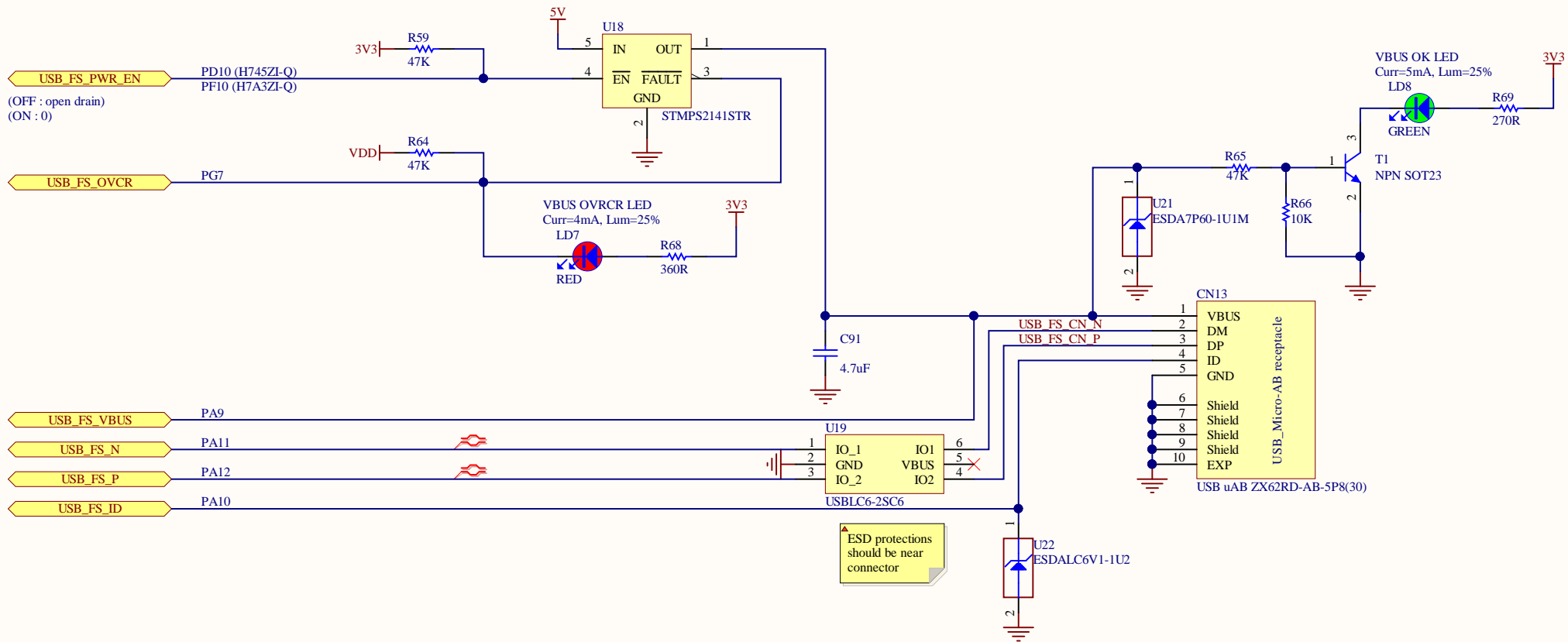
USER LED 3



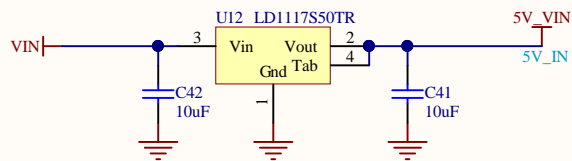
ETHERNET
only fitted for H745



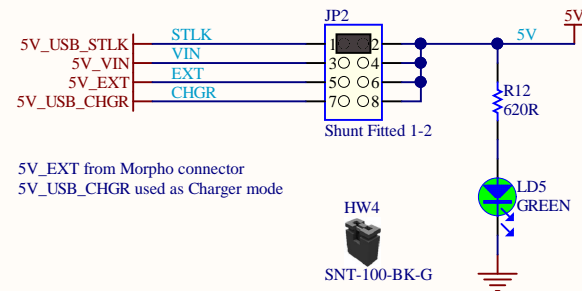
USB FS



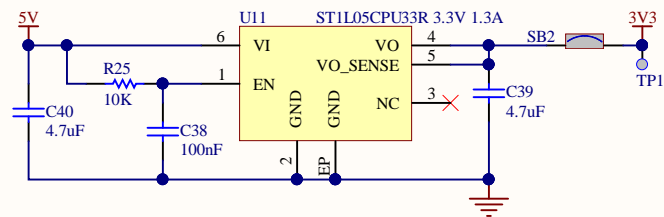
VIN / 5V PWR



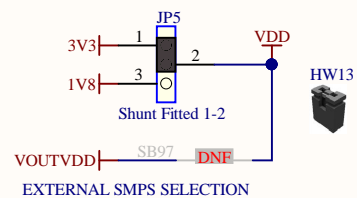
5V PWR SELECTION



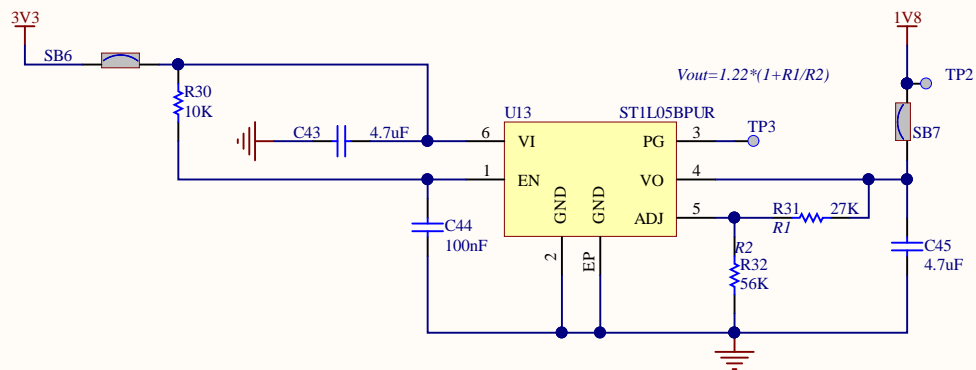
3V3 PWR

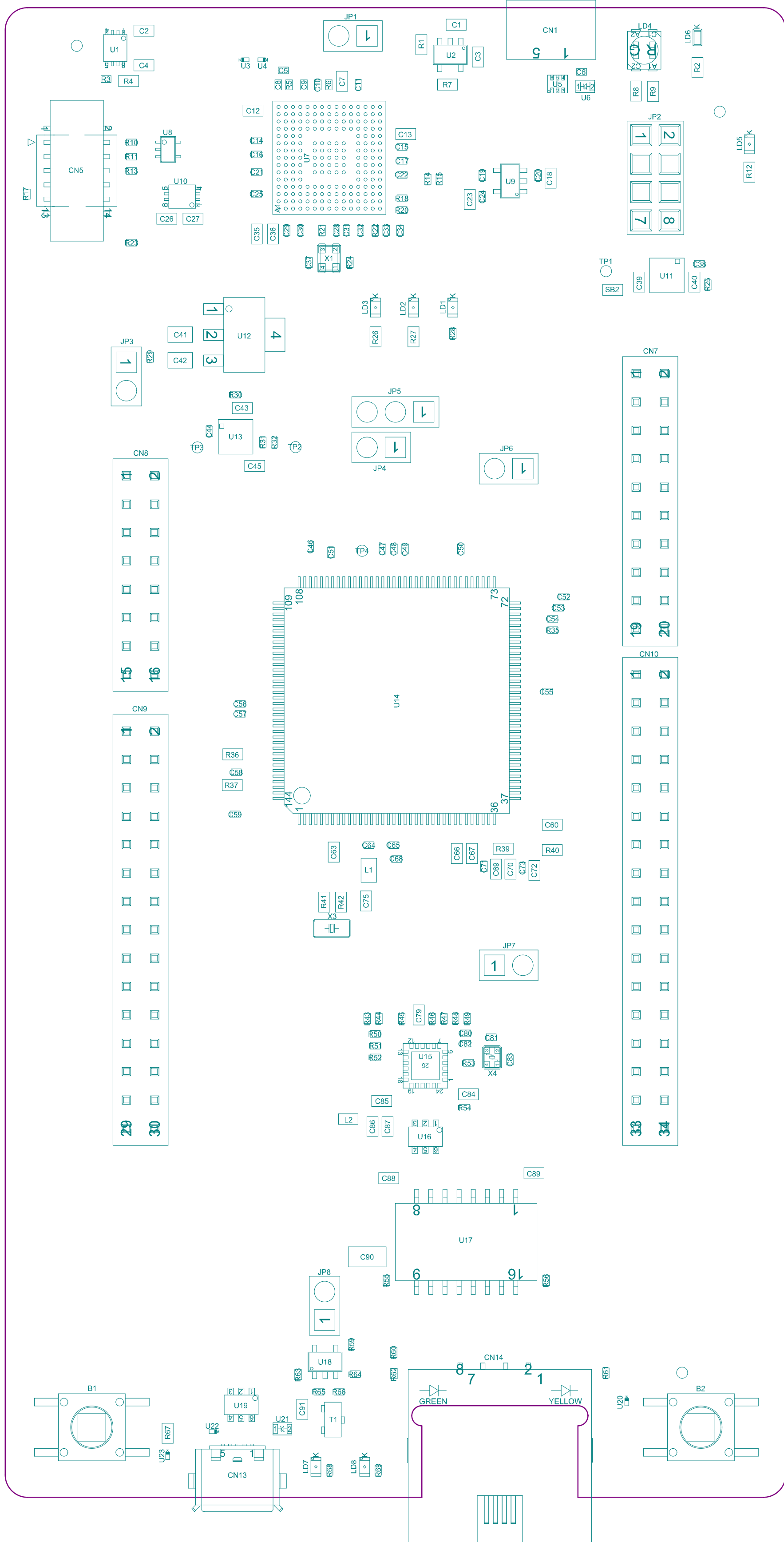


3V3/1V8 SELECTION



1V8 PWR





Project: Nucleo144 H7 SMPS with STLINK V3

Layer: M14-Top Assembly

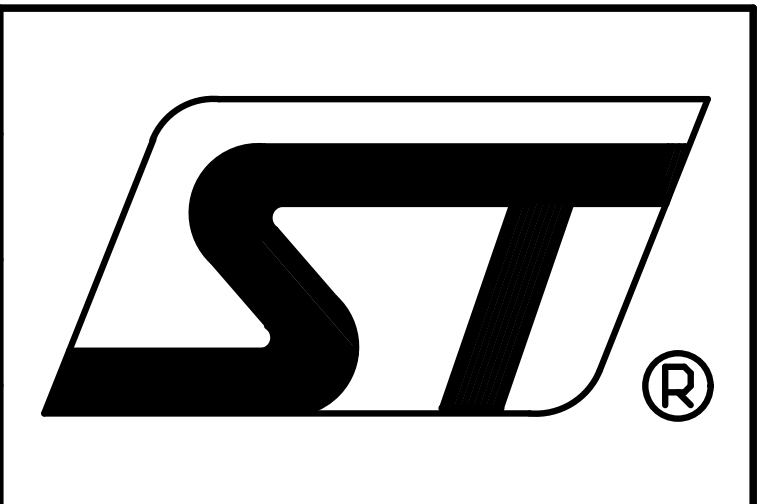
Gerber: .GM14

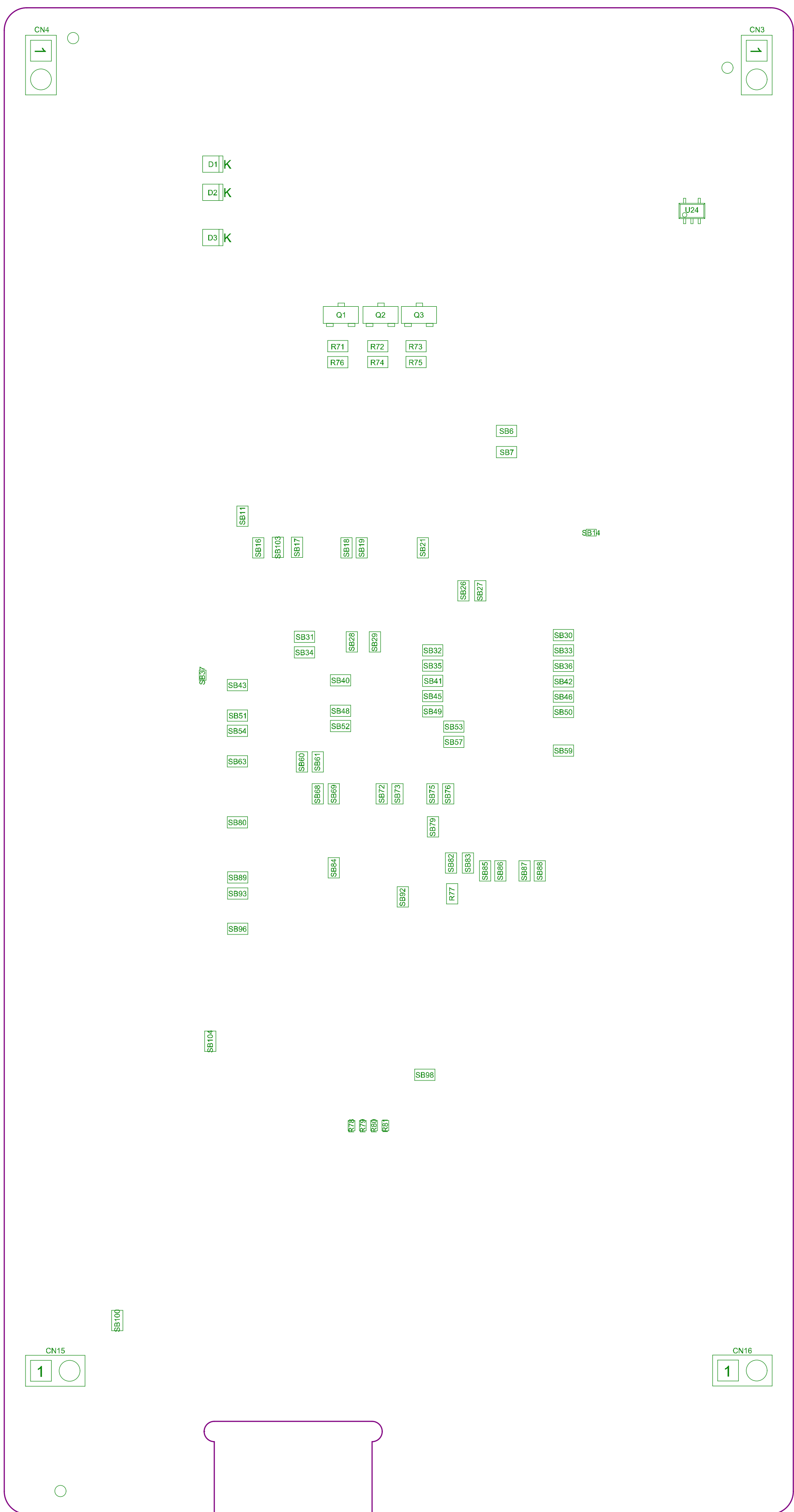
Variant: H755ZIQ

Ref: MB1363

Date: 09-OCT-19

Rev: D





Project: Nucleo144 H7 SMPS with STLINK V3	
Layer: M15-Bottom Assembly	Gerber: .GM15
Variant: H755ZIQ	Ref: MB1363
Date: 09-OCT-19	Rev: D

