3.23 Delay block (DLYB)

The delay block (DLYB) is used to generate an output clock dephased from the input clock. The phase of the output clock must be programmed by the user application. The output clock is then used to clock the data received by another peripheral such as an SDMMC or Octo-SPI interface. The delay is voltage and temperature dependent, that may require the application to re-configure and recenter the output clock phase with the received data.

The delay block main features are:

- Input clock frequency ranging from 25 to 250 MHz
- Up to 12 oversampling phases

3.24 Analog-to-digital converter (ADC1 and ADC2)

The devices embed two successive approximation analog-to-digital converters.

Table 5. ADC features

Mode/feature	ADC1	ADC2
Resolution	12 bit	
Maximum sampling speed	5 Msps (12-bit resolution)	
Dual mode operation	X	
Hardware offset calibration	X	
Hardware linearity calibration	-	
Single-end input	X	
Differential input	X	
Injected channel conversion	X	
Oversampling	Up to x256	
Data register	16 bits	
Data register FIFO depth	3 stages	
DMA support	X	
Parallel data output to ADF	-	
Offset compensation	X	
Gain compensation	-	
Number of analog watchdogs	3	
Option register		X

3.24.1 Analog temperature sensor

This sensor generates a voltage (V_{SENSE}) that varies linearly with temperature. It is internally connected to an ADC input channel used to convert the output voltage into a digital value.