

Reliability Evaluation Report

MDG-MCD-RER1815

STM32H72x / H73x (483x66)

New Product Qualification

General Information	
Commercial Product	STM32H72x / STM32H73x
Product Line	483X66
Die revision	483XXXZ (Cut 1.1)
Product Description	STM32H72x / H73x
Package	LQFP24x24 176L, LQFP20x20 144L, LQFP14x14 100L, UFBGA10x10 176L, UFBGA7x7 169L & 144L, TFBGA8x8 100L, VFQFPN8x8 68L, WLCSP115
Silicon Technology	CMOSM40 40nm <i>ST Crolles 300</i>
Division	MDG-MCD
Reliability Maturity Level	20->30

Traceability	
Diffusion Plant	<i>ST Crolles 300, France</i>
Assembly Plant	ASEKH. AMKOR ATP3, Philippines JSCC China AMKOR ATT1, Taiwan
Reliability Assessment	
Pass	<input checked="" type="checkbox"/>
Fail	<input type="checkbox"/>
Investigation required	<input type="checkbox"/>

Note: this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).

Version	Date	Author	Function
1.1	16 th May 2022	Jean-Marc BARBAROUX	MDG-MCD-Q&R Engineer
1.0	24 th Jun 2020	Jean-Marc BARBAROUX	MDG-MCD-Q&R Engineer

APPROVED BY:

Function	Location	Name	Date
Approval List Document revision 1.0			
Division Q&R Responsible	Rousset	Dominique GALIANO	06 th July 2020
Division Quality Manager	Rousset	Pascal NARCHE	07 th July 2020
Approval List Document revision 1.1			
Division Q&R Responsible	Rousset	Dominique GALIANO	17 th May 2022

TABLE OF CONTENTS

1	RELIABILITY EVALUATION OVERVIEW	4
1.1	OBJECTIVE	4
1.2	RELIABILITY STRATEGY	5
1.3	CONCLUSION	7
2	PRODUCT OR TEST VEHICLE CHARACTERISTICS.....	8
2.1	GENERALITIES.....	8
2.2	TRACEABILITY	8
2.2.1	<i>Wafer fab information.....</i>	<i>8</i>
2.2.2	<i>Assembly information</i>	<i>10</i>
2.2.3	<i>Reliability testing</i>	<i>15</i>
3	TESTS RESULTS SUMMARY	16
3.1	LOT INFORMATION	16
3.2	TEST PLAN AND RESULTS SUMMARY	17
4	APPLICABLE AND REFERENCE DOCUMENTS.....	24
5	GLOSSARY	25
6	REVISION HISTORY	25

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation on STM32H72x/H73x – Die 483XXXZ.

Test vehicle is described here below:

Product	Process, Package	Diffusion, Assembly plant	Comments
STM32H7251GT6	CMOS M40, LQFP 24x24 176L	ST Crolles 300, ASE KH	LQFP176 SMPS
STM32H725ZGT6	CMOS M40, LQFP 20x20 144L	ST Crolles 300, ASE KH	LQFP144 SMPS
STM32H723ZGT6	CMOS M40, LQFP 20x20 144L	ST Crolles 300, ASE KH	LQFP144 Legacy
STM32H725VGT6	CMOS M40, LQFP 14x14 100L	ST Crolles 300, ASE KH	LQFP100 SMPS
STM32H723VGT6	CMOS M40, LQFP 14x14 100L	ST Crolles 300, ASE KH	LQFP100 Legacy
STM32H7251GK6	CMOS M40, UFBGA10x10 176L	ST Crolles 300, ASE KH	UFBGA176 SMPS
STM32H725AGI6	CMOS M40, UFBGA7x7 169L	ST Crolles 300, ASE KH	UFBGA169 SMPS
STM32H723ZGI6	CMOS M40, UFBGA7x7 144L	ST Crolles 300, ASE KH	UFBGA144 Legacy
STM32H725VGH6	CMOS M40, TFBGA8x8 100L	ST Crolles 300, ATP3	TFBGA100 SMPS
STM32H723VGH6	CMOS M40, TFBGA8x8 100L	ST Crolles 300, ATP3	TFBGA100 Legacy
STM32H725RGV6	CMOS M40, VFQFPN 8x8 68L	ST Crolles 300, JSCC	VFQFN68 SMPS
STM32H725VGY6	CMOS M40, WLCSP 115L	ST Crolles 300, ATT1	CSP115 SMPS

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Reliability Strategy

The STM32H72x / H73x – Die 483XXXZ, is processed in the CMOS M40 process from ST Crolles 300 plant which is qualified through STM32H7xx 2M – Die 450 (RERMCD1401) for our division.

All following packages used for this product are qualified at division level for this product family.

Package	Reference	Assy Plant location
LQFP 24x24 176L (Gold wire)	RERMCD1401	ASE Kaohsiung Taiwan
LQFP 20x20 144L (Gold wire)	RERMCD1810	ASE Kaohsiung Taiwan
LQFP 14x14 100L (Gold wire)	RERMCD1810	ASE Kaohsiung Taiwan
UFBGA10x10 176L (Gold wire)	RERMCD1901	ASE Kaohsiung Taiwan
UFBGA7x7 169L (Gold wire)	RERMCD1901	ASE Kaohsiung Taiwan
UFBGA7x7 144L (Gold wire)	RERMCD1901	ASE Kaohsiung Taiwan
TFBGA8x8 100L (Gold wire)	RERMCD1617	AMKOR ATP3 Philippines
VFQFPN 8x8 68L (Gold wire)	RERMCD2013	JSCC China
WLCSP115	RERMCD1401	AMKOR ATT1 Taiwan

Based on these data, and according to “RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION” specification (DMS 0061692), the following qualification strategy has been defined:

- Die Qualification:
 - Cut1.0: 1 reliability lots to assess the die in UFBGA176 package.
 - Cut1.1: 1 reliability lot to assess the die in UFBGA176 package.

- Package Qualification:

The reliability test plan and result summary are presented in the following tables:

Package	Body	Pitch	Package Code	Wire	Assy	Bounding Option	Trial
LQFP 176	24x24	0.5	1T	Gold	ASEKH	SMPS	1 reliability lot
LQFP 144	20x20	0.5	1A	Gold	ASEKH	SMPS	1 reliability lot
LQFP 144	20x20	0.5	1A	Gold	ASEKH	Legacy	CDM
LQFP 100	14x14	0.5	1L	Gold	ASEKH	SMPS	CDM
LQFP 100	14x14	0.5	1L	Gold	ASEKH	Legacy	CDM
UFPGA 176	10x10	0.65	MR	Gold	ASEKH	SMPS	1 reliability lot
UFPGA 169	7x7	0.5	OQ	Gold	ASEKH	SMPS	CDM
UFPGA 144	7x7	0.5	OL	Gold	ASEKH	Legacy	CDM
TFPGA 100	8x8	0.8	DY	Gold	ATP3	SMPS	1 reliability lot
TFPGA 100	8x8	0.8	DY	Gold	ATP3	Legacy	CDM
VFQFPN 68	8x8	0.4	GB	Gold	JSCC	SMPS	3 reliability lots
WLCSP 115	-	0.35	GY	-	ATT1	SMPS	1 reliability lot

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for the STM32H72x / H73x – Die 483XXXZ in all packages listed in section 1.2

Refer to Section 3.0 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

The STM32H72x / H73x die 483XXXZ included Cortex–M7 in CMOS40 technology (40nm). It embeds a Flash memory up to 1 Mbytes, 564 Kbytes SRAM and additional features.

For additional information concerning the product behavior, refer to STM32H72x/H73x datasheet.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
FAB1	
Wafer fab name / location	ST Crolles 300 / France
Wafer diameter (inches)	12
Wafer thickness (µm)	775 +/- 25
Silicon process technology	CMOS40 40nm
Number of masks	51
Die finishing front side (passivation) materials/thicknesses	PSG + NITRIDE (1.1 µm)
Die finishing back side	RAW SILICON
Die area (Stepping die size) (µm)	3753, 4175
Die pad size (X,Y) (µm)	Bond pad 54.9, 54.4
Sawing street width (X,Y) (µm)	80,80
Metal levels/Materials/Thicknesses	Metal 1 Cu 0.130 µm Metal 2 Cu 0.140 µm Metal 3 Cu 0.140 µm Metal 4 Cu 0.140 µm Metal 5 Cu 0.140 µm Metal 6 Cu 1.000 µm Metal 7 Cu 1.000 µm Metal 8 Ta/TaN/AlCu 1.450 µm
Die over coating (material/thickness)	No
FIT level (Ea=0.7eV, C.L: 60%, 55°C)	3.1 FITs at qualification date

Soft Error Rate – Alpha SER [FIT/Mb] – Neutron SER [FIT/Mb] – Conditions	Alpha SER: 470 Fit/Mb. Alpha SER is estimated using a nominal flux of 0.001 α /h/cm ² Neutron SER: 900 Fit/Mb Neutron SER is an estimation at sea level of NYC (13n/h/cm ²)
Wafer Level Reliability – Electro–Migration (EM) – Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) – Hot Carrier Injection (HCI) – Negative Bias Thermal Instability (NBTI) – Stress Migration (SM)	Yes
Other Device(s) using same process	STM32H74x/H75x, die450

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1 – 1T LQFP 176 24X24X1.4	
Assembly plant name / location	ASEKH – TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/-25
Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	LF# A25472-0 LQ1 76L DR Pur tin C7025 SLOT PWB 6sq
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076WA
Wire bonding material/diameter/supplier	GOLD WIRE 0.8MIL
Molding compound material/supplier/reference	SUMITOMO EME-G631SH
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 2 – 1A LQFP 144 20X20X1.4	
Assembly plant name / location	ASEKH – TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/-25
Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	LF# A26746 PB LQ20 144 PureTin C7025 6.4sq 5.492ef
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076WA
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Molding compound material/supplier/reference	SUMITOMO EME-G631SH
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Package 3 – 1L LQFP 100 14x14x1.4	
Assembly plant name / location	ASEKH – TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/-25
Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	LF# A26886 PB LQ14 100 Pure Tin C7025
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076WA
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Molding compound material/supplier/reference	SUMITOMO EME–G631SH
Package Moisture Sensitivity Level (JEDEC J–STD020D)	MSL 3
Package 4 – MR UFBGA 176 +25 10x10x0.6	
Assembly plant name / location	ASEKH – TAIWAN
Pitch (mm)	0.65
Die thickness after back-grinding (µm)	75 +/-10
Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	SUBSTRATE UFBGA 10x10 176–25 483 ASE A26935
Die attach material/type(glue/film)/supplier	D/A Tape ABLESTICK ATB–125
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Balls metallurgy/diameter/supplier (BGA/CSP)	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Molding compound material/supplier/reference	KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J–STD020D)	MSL 3

Package 5– OQ UFBGA 169 7x7x0.6	
Assembly plant name / location	ASEKH – TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75 +/-10
Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	SUBSTRATE UFBGA 7x7 169L 483 ASE A26880
Die attach material/type(glue/film)/supplier	D/A Tape ABLESTICK ATB-125
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Balls metallurgy/diameter/supplier (BGA/CSP)	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Molding compound material/supplier/reference	KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 6– L4 UFBGA 144 7x7x0.6	
Assembly plant name / location	ASEKH – TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75 +/-10
Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	SUBSTRATE UFBGA 7x7 144L 483 ASE A26879
Die attach material/type(glue/film)/supplier	D/A Tape ABLESTICK ATB-125
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Balls metallurgy/diameter/supplier (BGA/CSP)	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Molding compound material/supplier/reference	KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Package 7 – DY TFBGA 100 8x8x0.8	
Assembly plant name / location	AMKOR ATP3
Pitch (mm)	0.8
Die thickness after back-grinding (µm)	180 +/- 15
Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	subs TFBGA 8x8 100 P0.8 SID 101411013
Die attach material/type(glue/film)/supplier	ABLEBOND GLUE 2300
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Balls metallurgy/diameter/supplier (BGA/CSP)	SOLDER BALL SAC 105 DIAM 0.35 MM
Molding compound material/supplier/reference	MOLDING COMPOUND GE100LFCS
Package Moisture Sensitivity Level (JEDEC J–STD020D)	MSL 3
Package 8 – GB VFQFPN 8x8x1 68L P0.4	
Assembly plant name / location	SC–StatsChippac–China (SCCJ)
Pitch (mm)	0.4
Die thickness after back-grinding (µm)	254±25
Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	LF VQFN68L 8x8Std Rough Cu Ag plating JSCC 054009L
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	Glue Hitachi EN4900GC
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Molding compound material/supplier/reference	SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J–STD020D)	MSL 3
Package 9 – JF WLCSP 115L P0.35 DIE 483	
Assembly plant name / location	SC AMKOR ATT1 – TAIWAN
Pitch (mm)	0.35
Die thickness after back-grinding (µm)	355 +/-25

Die sawing method	Laser Grooving + Mechanical sawing
Bill of Material elements	
Balls metallurgy/diameter/supplier (BGA/CSP)	Solder ball SAC405 Diam 220um
Routing/Redistribution layer (RDL) material (CSP)	Copper 6um
PBO passivation material (CSP)	Passivation HD8820
Backside coating material/thickness (CSP)	Back side coating PET film
Package Moisture Sensitivity Level (JEDEC J–STD020D)	MSL 1

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	RSST / ST Rousset GRAL / ST Grenoble

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.

ST certification document can be downloaded under the following link:

http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot	Die Revision (Cut)	Trace Code	Raw Line	Package	Note
1	VQ911328	1.0	AA934001	E0MR*483ESXA	ASEKH UFBGA 176	Die & Package assessment
2	VQ911328	1.1	AA007090	E0MR*483ESXZ	ASEKH UFBGA 176	Die assessment
3	VQ911328	1.0	AA936056	E01T*483ESXA	ASEKH LQFP 176 SMPS	Package assessment
4	VQ911328	1.0	AA935003	E01A*483ESXA	ASEKH LQFP 144 SMPS	Package assessment
5	VQ911328	1.0	AA933101	E21A*483ESXA	ASEKH LQFP 144 Legacy	Package assessment
6	VQ911328	1.0	AA935001	E01L*483ESXA	ASEKH LQFP 100 SMPS	Package assessment
7	VQ913599	1.0	AA940053	E11L*483XXXA	ASEKH LQFP 100 Legacy	Package assessment
8	VQ911328	1.0	AA934134	E0OQ*483XXXA	ASEKH UFBGA 169 SMPS	Package assessment
9	VQ911328	1.0	AA934136	E0L4*483ESXA	ASEKH UFBGA 144 Legacy	Package assessment
10	VQ911328	1.0	7B933A8Y	P1DY*483ESXA	ATP3 TFBGA 100 SMPS	Package assessment
11	VQ911328	1.0	7B933A8Z	PODY*483ESXA	ATP3 TFBGA 100 Legacy	Package assessment
12	VQ911328	1.0	A593700B	TOJF*483ESXA	ATTT1 WLCSP 115 SMPS	Package assessment
13	VQ913599	1.0	GQ94425L	70GB*483ESXA	JSCC VQFN 68 SMPS	Package assessment
14	VQ913599	1.0	GQ9462BH	70GB*483ESXA	JSCC VQFN 68 SMPS	Package assessment
15	VQ913599	1.0	GQ9452AO	70GB*483ESXA	JSCC VQFN 68 SMPS	Package assessment

3.2 Test plan and results summary

Table 5 – ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Tj=140°C Duration= 1200H 3V6	2	77	154	Lot1: 0/77 Lot2: 0/77	
ELFR	JESD22-A108 JESD74	Tj=140°C Duration= 48H 3V6	2	500	1000	Lot1: 0/500 Lot2: 0/500	
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF <u>SMPS version</u> 1kV class1C (1KV VFBSMPS pin, others 2KV) <u>Legacy version</u> 2kV class 2	2	3	6	Lot1: 0/3 Lot2: 0/3	
LatchUp	JESD78	Tj = 140°C	2	3	6	Lot1: 0/3 Lot2: 0/3	
EDR	JESD22-A117	10kcy EW @ 140°C Tj then Storage HTB 150°C - Duration 1500H	2	77	154	Lot1: 0/77 Lot2: 0/77	
EDR	JESD22-A117	10kcy EW @ 25°C Ta then Storage HTB 150°C - Duration 168H	2	77	154	Lot1: 0/77 Lot2: 0/77	
EDR	JESD22-A117	10kcy EW @ -40°C Ta then Storage HTB 150°C - Duration 168H	2	77	154	Lot1: 0/77 Lot2: 0/77	

Table 6 - ACCELERATED ENVIRONMENT STRESS TESTS

LQFP24x24 176L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	1	3	3	Lot3: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot3: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc <input checked="" type="checkbox"/> After PC	1	77	77	Lot3: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H <input checked="" type="checkbox"/> After PC	1	77	77	Lot3: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000H <input checked="" type="checkbox"/> After PC	1	77	77	Lot3: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 <input checked="" type="checkbox"/> After PC	1	77	77	Lot3: 0/77	

LQFP20x20 144L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	1	3	3	Lot4: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot4: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc <input checked="" type="checkbox"/> After PC	1	77	77	Lot4: 0/77	

UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H <input checked="" type="checkbox"/> After PC	1	77	77	Lot4: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000H <input checked="" type="checkbox"/> After PC	1	77	77	Lot4: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 <input checked="" type="checkbox"/> After PC	1	77	77	Lot4: 0/77	

LQFP20x20 144L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	1	3	3	Lot5: 0/3	

LQFP14x14 100L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	1	3	3	Lot6: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot6: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc <input checked="" type="checkbox"/> After PC	1	77	77	Lot6: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H <input checked="" type="checkbox"/> After PC	1	77	77	Lot6: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000H <input checked="" type="checkbox"/> After PC	1	77	77	Lot6: 0/77	

THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 <input checked="" type="checkbox"/> After PC	1	77	77	Lot6: 0/77	
-----	--------------	--	---	----	----	------------	--

LQFP14x14 100L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	1	3	3	Lot7: 0/3	

UFBGA10X10 176L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	2	3	6	Lot1: 0/3 Lot2: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot1: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc <input checked="" type="checkbox"/> After PC	1	77	77	Lot1: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H <input checked="" type="checkbox"/> After PC	1	77	77	Lot1: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000H <input checked="" type="checkbox"/> After PC	1	77	77	Lot1: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 <input checked="" type="checkbox"/> After PC	1	77	77	Lot1: 0/77	

UFPGA7X7 169L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot8: 0/3	

UFPGA7X7 144L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot9: 0/3	

TFBGA8X8 100, ATP3

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot10: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot10: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc <input checked="" type="checkbox"/> After PC	1	77	77	Lot10: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H <input checked="" type="checkbox"/> After PC	1	77	77	Lot10: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000H <input checked="" type="checkbox"/> After PC	1	77	77	Lot10: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 <input checked="" type="checkbox"/> After PC	1	77	77	Lot10: 0/77	

TFBGA8X8 100L, ATP3

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot11: 0/3	

WLCSP115 115, ATT1

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot12: 0/3	
PC	J-STD-020	24h bake@125°C, MSL1 (168H 85°C 85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot12: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc <input checked="" type="checkbox"/> After PC	1	77	77	Lot12: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H <input checked="" type="checkbox"/> After PC	1	77	77	Lot12: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000H <input checked="" type="checkbox"/> After PC	1	77	77	Lot12: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 <input checked="" type="checkbox"/> After PC	1	77	77	Lot12: 0/77	

VQFN 8x8 68L, JSCC (RERMCD2013)

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot13: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	3	256	768	Lot13: 0/256 Lot14: 0/256 Lot15: 0/256	

TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc <input checked="" type="checkbox"/> After PC	3	77	231	Lot 13: 0/77 Lot 14: 0/77 Lot 15: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs <input checked="" type="checkbox"/> After PC	3	77	231	Lot 13: 0/77 Lot 14: 0/77 Lot 15: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs <input checked="" type="checkbox"/> After PC	3	77	231	Lot 13: 0/77 Lot 14: 0/77 Lot 15: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 <input checked="" type="checkbox"/> After PC	3	25	75	Lot 13: 0/25 Lot 14: 0/25 Lot 15: 0/25	

Note: Test method revision reference is the one active at the date of reliability trial execution

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A117	Endurance and Data retention
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A110:	Temperature Humidity Bake
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension

5 GLOSSARY

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HAST	Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.1	Jean-Marc BARBAROUX	Typo error Table4 VQFN64 has been replaced by VQFN68	Q&R Quality Manager	Rousset	Dominique GALIANO	17 th May 2022
1.0	Jean-Marc BARBAROUX	Initial release	Div. Quality Manager	Rousset	Pascal NARCHE	07 th July 2020
			Q&R Quality Manager	Rousset	Dominique GALIANO	06 th July 2020

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics International NV and its affiliates (“ST”) reserve the right to make changes corrections, enhancements, modifications, and improvements to ST products and/or to this document any time without notice.

This document is provided solely for the purpose of obtaining general information relating to an ST product. Accordingly, you hereby agree to make use of this document solely for the purpose of obtaining general information relating to the ST product. You further acknowledge and agree that this document may not be used in or in connection with any legal or administrative proceeding in any court, arbitration, agency, commission or other tribunal or in connection with any action, cause of action, litigation, claim, allegation, demand or dispute of any kind. You further acknowledge and agree that this document shall not be construed as an admission, acknowledgement or evidence of any kind, including, without limitation, as to the liability, fault or responsibility whatsoever of ST or any of its affiliates, or as to the accuracy or validity of the information contained herein, or concerning any alleged product issue, failure, or defect. ST does not promise that this document is accurate or error free and specifically disclaims all warranties, express or implied, as to the accuracy of the information contained herein. Accordingly, you agree that in no event will ST or its affiliates be liable to you for any direct, indirect, consequential, exemplary, incidental, punitive, or other damages, including lost profits, arising from or relating to your reliance upon or use of this document.

Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement, including, without limitation, the warranty provisions thereunder.

In that respect please note that ST products are not designed for use in some specific applications or environments described in above mentioned terms and conditions.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

Information furnished is believed to be accurate and reliable. However, ST assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously in any prior version of this document.

© 2022 STMicroelectronics - All rights reserved