
STM32
CubeMX

1. Description

1.1. Project

Project Name	ACIO_01_06_22
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	11/21/2022

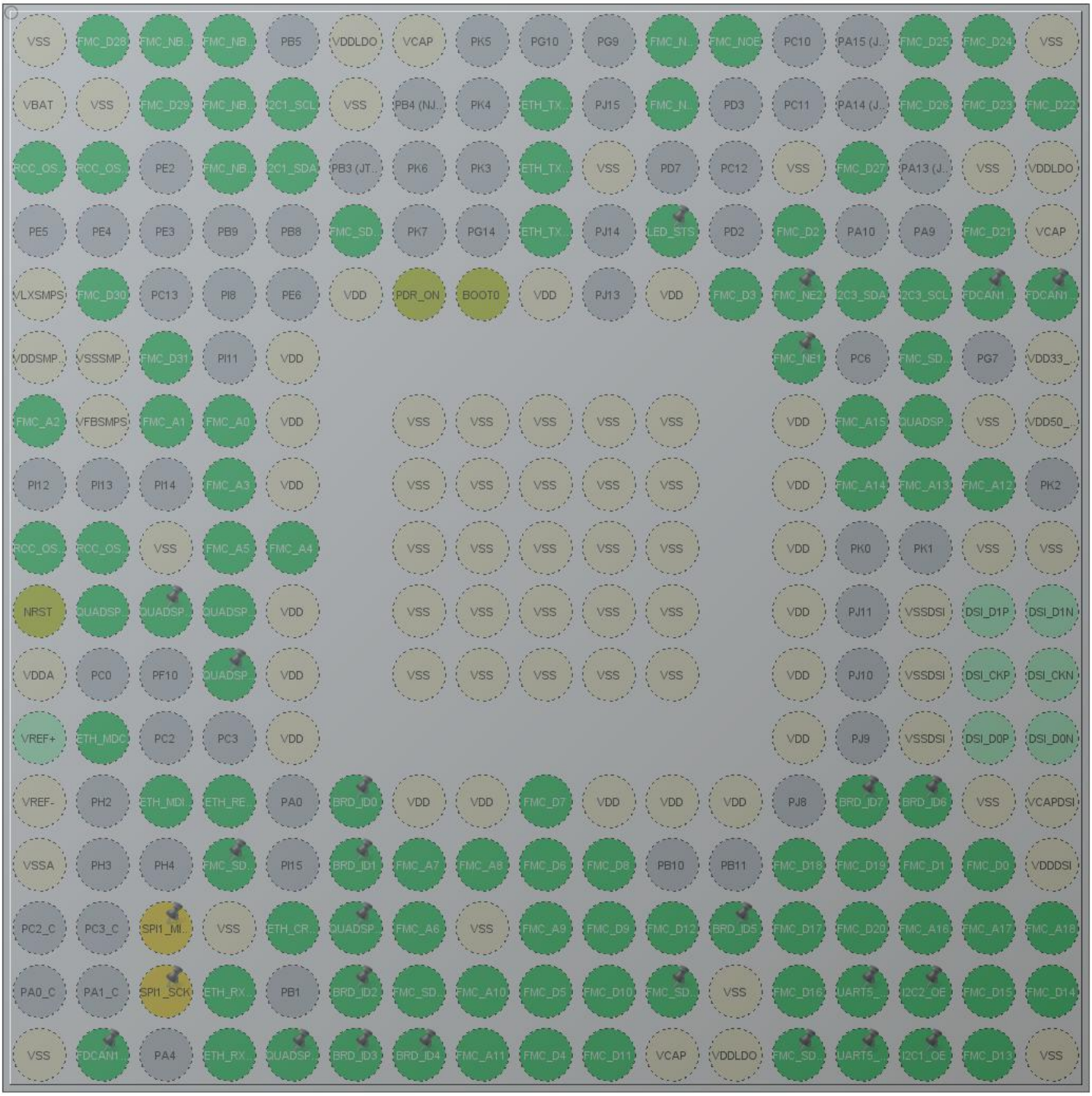
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H747/757
MCU name	STM32H747XIHx
MCU Package	TFBGA240
MCU Pin number	265

1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4

2. Pinout Configuration



TFBGA240 +25 (Top view)

3. Pins Configuration

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PI6	I/O	FMC_D28	
A3	PI5	I/O	FMC_NBL3	
A4	PI4	I/O	FMC_NBL2	
A6	VDDLDO	Power		
A7	VCAP	Power		
A11	PD5	I/O	FMC_NWE	
A12	PD4	I/O	FMC_NOE	
A15	PI1	I/O	FMC_D25	
A16	PI0	I/O	FMC_D24	
A17	VSS	Power		
B1	VBAT	Power		
B2	VSS	Power		
B3	PI7	I/O	FMC_D29	
B4	PE1	I/O	FMC_NBL1	
B5	PB6	I/O	I2C1_SCL	
B6	VSS	Power		
B9	PG11	I/O	ETH_TX_EN	
B11	PD6	I/O	FMC_NWAIT	
B15	PI2	I/O	FMC_D26	
B16	PH15	I/O	FMC_D23	
B17	PH14	I/O	FMC_D22	
C1	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
C2	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
C4	PE0	I/O	FMC_NBL0	
C5	PB7	I/O	I2C1_SDA	
C9	PG12	I/O	ETH_TXD1	
C10	VSS	Power		
C13	VSS	Power		
C14	PI3	I/O	FMC_D27	
C16	VSS	Power		
C17	VDDLDO	Power		
D6	PG15	I/O	FMC_SDNCAS	
D9	PG13	I/O	ETH_TXD0	

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
D11	PJ12 *	I/O	GPIO_Output	LED_STS
D13	PD0	I/O	FMC_D2	
D16	PH13	I/O	FMC_D21	
D17	VCAP	Power		
E1	VLXSMPS	Power		
E2	PI9	I/O	FMC_D30	
E6	VDD	Power		
E7	PDR_ON	Reset		
E8	BOOT0	Boot		
E9	VDD	Power		
E11	VDD	Power		
E12	PD1	I/O	FMC_D3	
E13	PC8	I/O	FMC_NE2	
E14	PC9	I/O	I2C3_SDA	
E15	PA8	I/O	I2C3_SCL	
E16	PA12	I/O	FDCAN1_TX	
E17	PA11	I/O	FDCAN1_RX	
F1	VDDSMPS	Power		
F2	VSSSMPS	Power		
F3	PI10	I/O	FMC_D31	
F5	VDD	Power		
F13	PC7	I/O	FMC_NE1	
F15	PG8	I/O	FMC_SDCLK	
F17	VDD33_USB	Power		
G1	PF2	I/O	FMC_A2	
G2	VFBSMPS	Power		
G3	PF1	I/O	FMC_A1	
G4	PF0	I/O	FMC_A0	
G5	VDD	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G11	VSS	Power		
G13	VDD	Power		
G14	PG5	I/O	FMC_A15, FMC_BA1	
G15	PG6	I/O	QUADSPI_BK1_NCS	
G16	VSS	Power		
G17	VDD50_USB	Power		

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H4	PF3	I/O	FMC_A3	
H5	VDD	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H11	VSS	Power		
H13	VDD	Power		
H14	PG4	I/O	FMC_A14, FMC_BA0	
H15	PG3	I/O	FMC_A13	
H16	PG2	I/O	FMC_A12	
J1	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
J2	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
J3	VSS	Power		
J4	PF5	I/O	FMC_A5	
J5	PF4	I/O	FMC_A4	
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J11	VSS	Power		
J13	VDD	Power		
J16	VSS	Power		
J17	VSS	Power		
K1	NRST	Reset		
K2	PF6	I/O	QUADSPI_BK1_IO3	
K3	PF7	I/O	QUADSPI_BK1_IO2	
K4	PF8	I/O	QUADSPI_BK1_IO0	
K5	VDD	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VSS	Power		
K13	VDD	Power		
K15	VSSDSI	Power		
L1	VDDA	Power		
L4	PF9	I/O	QUADSPI_BK1_IO1	
L5	VDD	Power		

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L7	VSS	Power		
L8	VSS	Power		
L9	VSS	Power		
L10	VSS	Power		
L11	VSS	Power		
L13	VDD	Power		
L15	VSSDSI	Power		
M2	PC1	I/O	ETH_MDC	
M5	VDD	Power		
M13	VDD	Power		
M15	VSSDSI	Power		
N1	VREF-	Power		
N3	PA2	I/O	ETH_MDIO	
N4	PA1	I/O	ETH_REF_CLK	
N6	PJ0 *	I/O	GPIO_Input	BRD_ID0
N7	VDD	Power		
N8	VDD	Power		
N9	PE10	I/O	FMC_D7	
N10	VDD	Power		
N11	VDD	Power		
N12	VDD	Power		
N14	PJ7 *	I/O	GPIO_Input	BRD_ID7
N15	PJ6 *	I/O	GPIO_Input	BRD_ID6
N16	VSS	Power		
N17	VCAPDSI	Power		
P1	VSSA	Power		
P4	PH5	I/O	FMC_SDNWE	
P6	PJ1 *	I/O	GPIO_Input	BRD_ID1
P7	PF13	I/O	FMC_A7	
P8	PF14	I/O	FMC_A8	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P13	PH10	I/O	FMC_D18	
P14	PH11	I/O	FMC_D19	
P15	PD15	I/O	FMC_D1	
P16	PD14	I/O	FMC_D0	
P17	VDDDSI	Power		
R3	PA6 **	I/O	SPI1_MISO	
R4	VSS	Power		

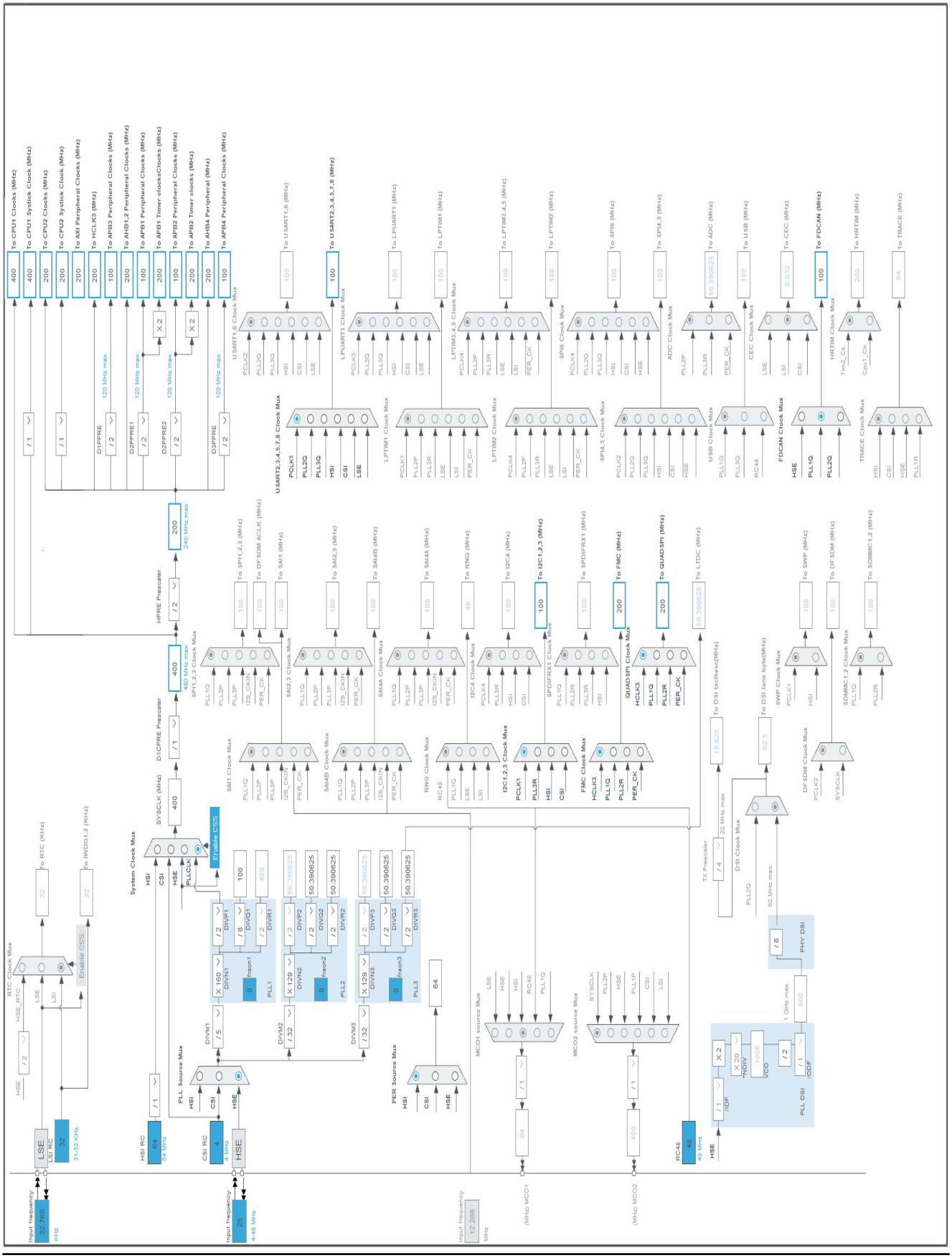
Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R5	PA7	I/O	ETH_CRS_DV	
R6	PB2	I/O	QUADSPI_CLK	
R7	PF12	I/O	FMC_A6	
R8	VSS	Power		
R9	PF15	I/O	FMC_A9	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PJ5 *	I/O	GPIO_Input	BRD_ID5
R13	PH9	I/O	FMC_D17	
R14	PH12	I/O	FMC_D20	
R15	PD11	I/O	FMC_A16	
R16	PD12	I/O	FMC_A17	
R17	PD13	I/O	FMC_A18	
T3	PA5 **	I/O	SPI1_SCK	
T4	PC4	I/O	ETH_RXD0	
T6	PJ2 *	I/O	GPIO_Input	BRD_ID2
T7	PF11	I/O	FMC_SDNRAS	
T8	PG0	I/O	FMC_A10	
T9	PE8	I/O	FMC_D5	
T10	PE13	I/O	FMC_D10	
T11	PH6	I/O	FMC_SDNE1	
T12	VSS	Power		
T13	PH8	I/O	FMC_D16	
T14	PB12	I/O	UART5_RX	
T15	PB15 *	I/O	GPIO_Output	I2C2_OE
T16	PD10	I/O	FMC_D15	
T17	PD9	I/O	FMC_D14	
U1	VSS	Power		
U2	PA3 *	I/O	GPIO_Output	FDCAN1_LBK
U4	PC5	I/O	ETH_RXD1	
U5	PB0 *	I/O	GPIO_Output	QUADSPI_RESET
U6	PJ3 *	I/O	GPIO_Input	BRD_ID3
U7	PJ4 *	I/O	GPIO_Input	BRD_ID4
U8	PG1	I/O	FMC_A11	
U9	PE7	I/O	FMC_D4	
U10	PE14	I/O	FMC_D11	
U11	VCAP	Power		
U12	VDDLDO	Power		
U13	PH7	I/O	FMC_SDCKE1	

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
U14	PB13	I/O	UART5_TX	
U15	PB14 *	I/O	GPIO_Output	I2C1_OE
U16	PD8	I/O	FMC_D13	
U17	VSS	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	ACIO_01_06_22
Project Folder	Z:\MyWork\SCT\ADE\ACIO_21_06_22
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_FDCAN1_Init	FDCAN1
4	MX_LWIP_Init	LWIP
5	MX_FMC_Init	FMC
6	MX_I2C1_Init	I2C1
7	MX_I2C3_Init	I2C3
8	MX_QUADSPI_Init	QUADSPI
9	MX_UART5_Init	UART5
10	MX_TIM2_Init	TIM2

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H747/757
MCU	STM32H747XIHx
Datasheet	DS12930_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

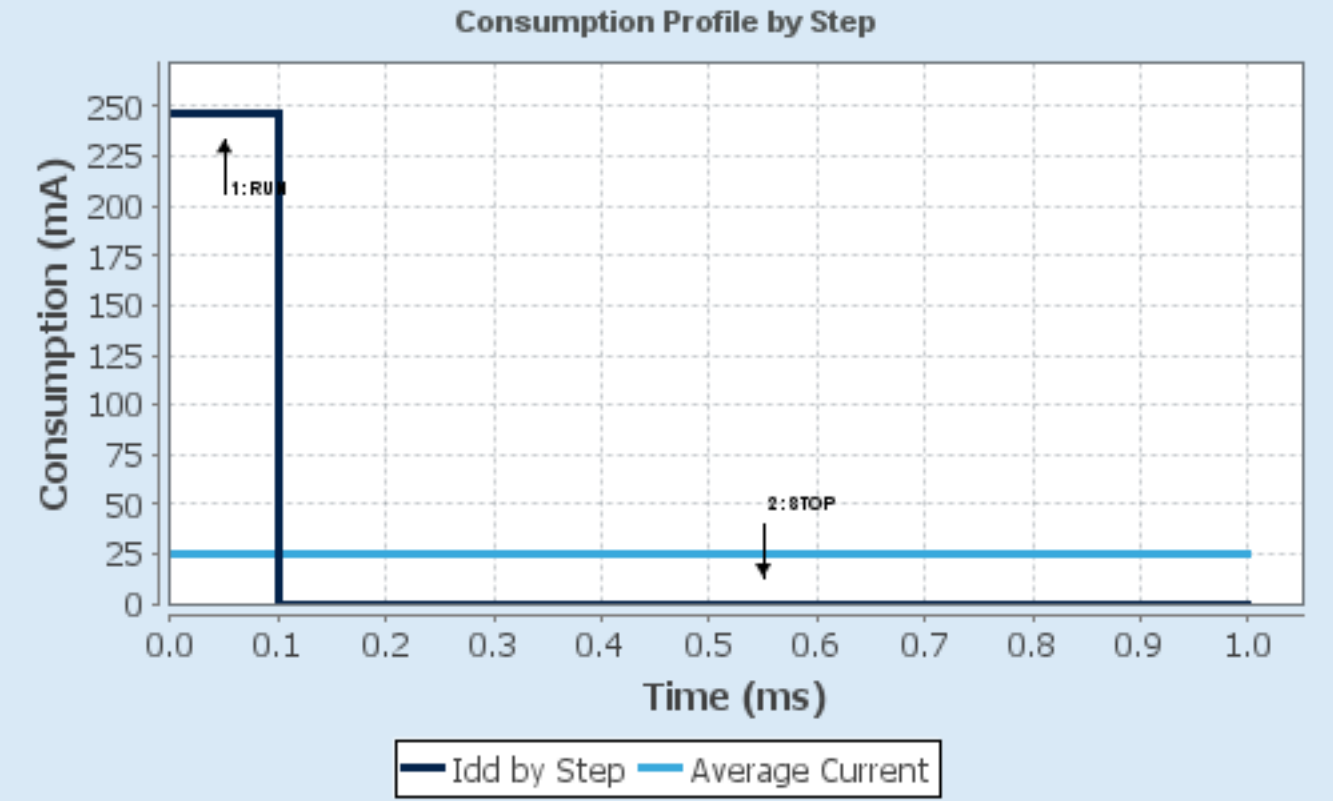
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_IPs_ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
250
225
200
175
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Cortex Interface Settings:

CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	**Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers ***

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x30000000 ***
MPU Region Size	**32KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	**ENABLE ***
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

7.2. ETH

Mode: RMII

7.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30000080 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30000000 ***
Rx Buffers Address	**0x30000100 ***

Rx Buffers Length	1524

7.3. FDCAN1

mode: Activated

7.3.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	**Enable ***
Transmit Pause	**Enable ***
Protocol Exception	Disable
Nominal Prescaler	**16 ***
Nominal Sync Jump Width	**16 ***
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	**4 ***
Data Time Seg1	**5 ***
Data Time Seg2	**4 ***
Message Ram Offset	0
Std Filters Nbr	**1 ***
Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	**1 ***
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	**1 ***
Tx Fifo Queue Mode	FIFO mode

Tx Elmt Size	8 bytes data field

7.4. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: SRAM

Address: 19 bits

Data: 32 bits

Wait: Asynchronous

Byte enable: 32-bit byte enable

NOR Flash/PSRAM/SRAM/ROM/LCD 2

Chip Select: NE2

Memory type: SRAM

Address: 19 bits

Data: 32 bits

Wait: Asynchronous

Byte enable: 32-bit byte enable

SDRAM 1

Clock and chip enable: SDCKE1+SDNE1

Internal bank number: 4 banks

Address: 12 bits

Data: 32 bits

Byte enable: 32-bit byte enable

7.4.1. NOR/PSRAM 1:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

NOR/PSRAM control:

Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 1
Write operation	**Enabled ***
Write FIFO	Enabled
Extended mode	**Enabled ***

Wait signal polarity	Low polarity

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	**3 ***
Data setup time in HCLK clock cycles	**4 ***
Bus turn around time in HCLK clock cycles	**1 ***
Access mode	A

NOR/PSRAM timing for write accesses:

Extended address setup time	**3 ***
Extended data setup time	**4 ***
Extended bus turn around time	**1 ***
Extended access mode	A

7.4.2. Bank Mapping:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Mapping parameters:

FMC bank mapping	Default mapping

7.4.3. NOR/PSRAM 2:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

NOR/PSRAM control:

Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 2
Write operation	**Enabled ***
Write FIFO	Enabled
Extended mode	**Enabled ***
Wait signal polarity	Low polarity

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	**3 ***

Data setup time in HCLK clock cycles	**4 ***
Bus turn around time in HCLK clock cycles	**1 ***
Access mode	A

NOR/PSRAM timing for write accesses:

Extended address setup time	**3 ***
Extended data setup time	**4 ***
Extended bus turn around time	**1 ***
Extended access mode	A

7.4.4. SDRAM 1:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

SDRAM control:

Bank	SDRAM bank 2
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**6 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**6 ***
Write recovery time	**2 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

7.5. I2C1

I2C: I2C

7.5.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. I2C3

I2C: I2C

7.6.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.7.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

General Parameters:

Clock Prescaler	**3 ***
Fifo Threshold	**4 ***
Sample Shifting	**Sample Shifting Half Cycle ***
Flash Size	**25 ***
Chip Select High Time	**2 Cycles ***
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7

	Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Product revision	rev.Y

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL1 clock Output range	Wide VCO range

7.9. SYS_M4

Timebase Source: SysTick

7.9.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

7.10. SYS

Timebase Source: SysTick

7.10.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

7.11. TIM2

Clock Source : Internal Clock

7.11.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**40000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**65536-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.12. UART5

Mode: Asynchronous

7.12.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.13. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.13.1. General Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	**Disabled ***

IP Address Settings:

IP_ADDRESS (IP Address)	**192.168.001.199 ***
NETMASK_ADDRESS (Netmask Address)	**255.255.255.000 ***
GATEWAY_ADDRESS (Gateway Address)	**192.168.001.001 ***

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Disabled

Platform Settings:

PHY Driver	Choose/LAN8742

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.13.2. Key Options:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Not Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	**10*1024 ***
LWIP_RAM_HEAP_POINTER (RAM Heap Pointer)	**0x30002000 ***

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled

TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Disabled

7.13.3. PPP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.13.4. IPv6:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.13.5. HTTPD:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

7.13.6. SNMP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.13.7. SNTP/SMTP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)	Disabled

7.13.8. MDNS/TFTP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.13.9. Perf/Checks:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.13.10. Statistics:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.13.11. Checksum:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Enabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled

CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Enabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.13.12. Debug:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

7.13.13. Platform Settings:

Driver_PHY	LAN8742

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
ETH	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PG12	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
FDCAN1	PA12	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PA11	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
FMC	PI6	FMC_D28	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI5	FMC_NBL3	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI4	FMC_NBL2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI1	FMC_D25	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI0	FMC_D24	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI7	FMC_D29	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PD6	FMC_NWAIT	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI2	FMC_D26	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH15	FMC_D23	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH14	FMC_D22	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI3	FMC_D27	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH13	FMC_D21	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI9	FMC_D30	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PC8	FMC_NE2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PI10	FMC_D31	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PC7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG5	FMC_A15	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG4	FMC_A14	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG3	FMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG2	FMC_A12	Alternate Function	No pull-up and no pull-	Very High		Cortex-M7	D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down				
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH10	FMC_D18	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH11	FMC_D19	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH9	FMC_D17	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH12	FMC_D20	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD11	FMC_A16	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD12	FMC_A17	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD13	FMC_A18	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH8	FMC_D16	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH7	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-M7	D2
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-M7	D2
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-M7	D2
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-M7	D2
QUADSPI	PG6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PF6	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PF7	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PF8	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PF9	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
RCC	PC15-	RCC_OSC32	n/a	n/a	n/a		Cortex-M7*	D3

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	OSC32_OUT	_OUT					Cortex-M4	
	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
UART5	PB12	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PB13	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
Single Mapped Signals	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low			
GPIO	PJ12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_STS		
	PJ0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRD_ID0		
	PJ7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRD_ID7		
	PJ6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRD_ID6		
	PJ1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRD_ID1		
	PJ5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRD_ID5		
	PJ2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRD_ID2		
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	I2C2_OE		
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FDCAN1_LBK		
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	QUADSPI_RESET		
	PJ3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRD_ID3		
	PJ4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRD_ID4		
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	I2C1_OE		

* Initialized context

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FDCAN1 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
FMC global interrupt	unused		
UART5 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FDCAN calibration unit interrupt	unused		
CM4 send event interrupt for CM7	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
QUADSPI global interrupt	unused		
HSEM1 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

8.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

8.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
CM7 send event interrupt for CM4	unused		
FPU global interrupt	unused		
HSEM2 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

8.5.4. NVIC2 Code generation

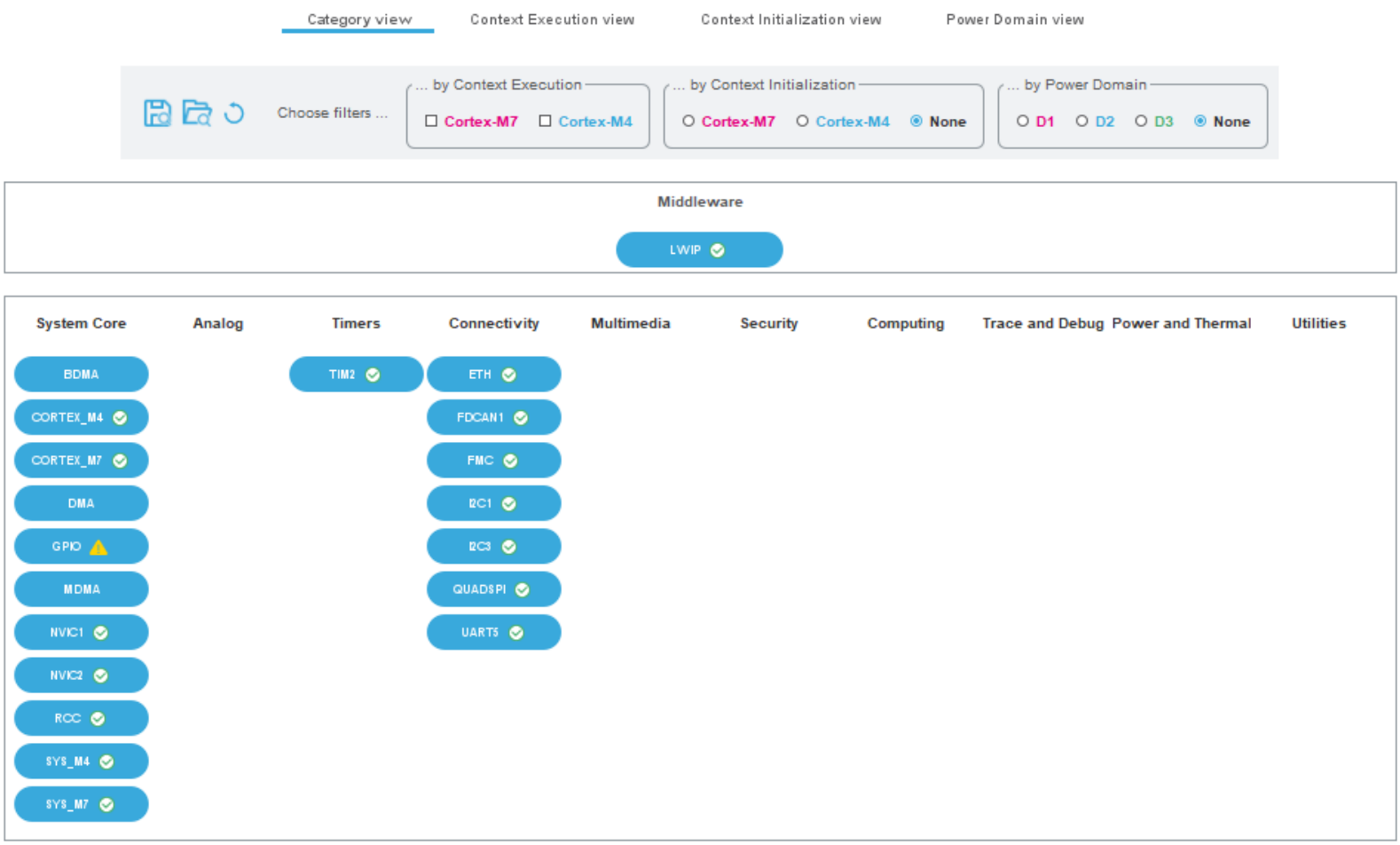
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

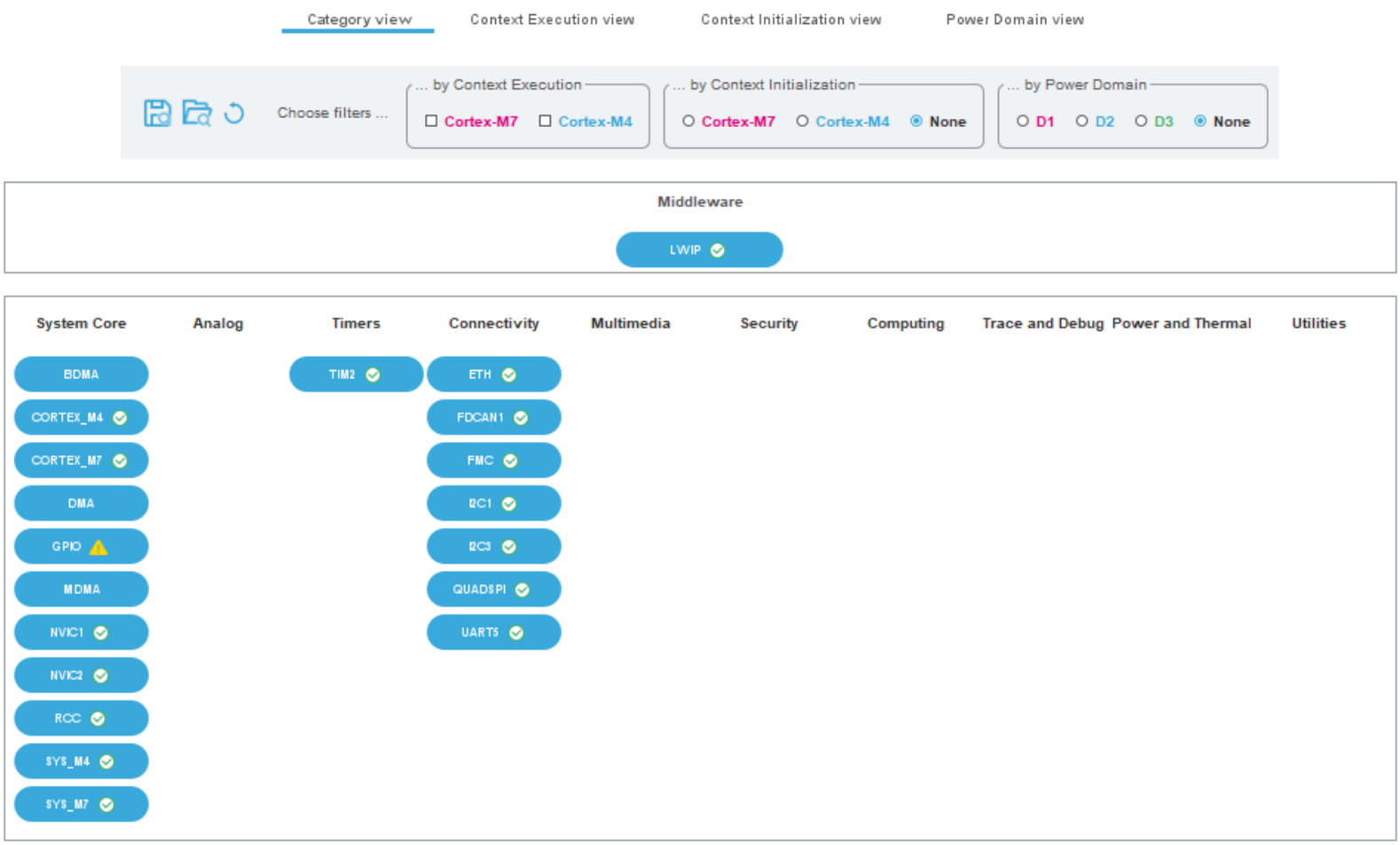
9. System Views

9.1. Category view

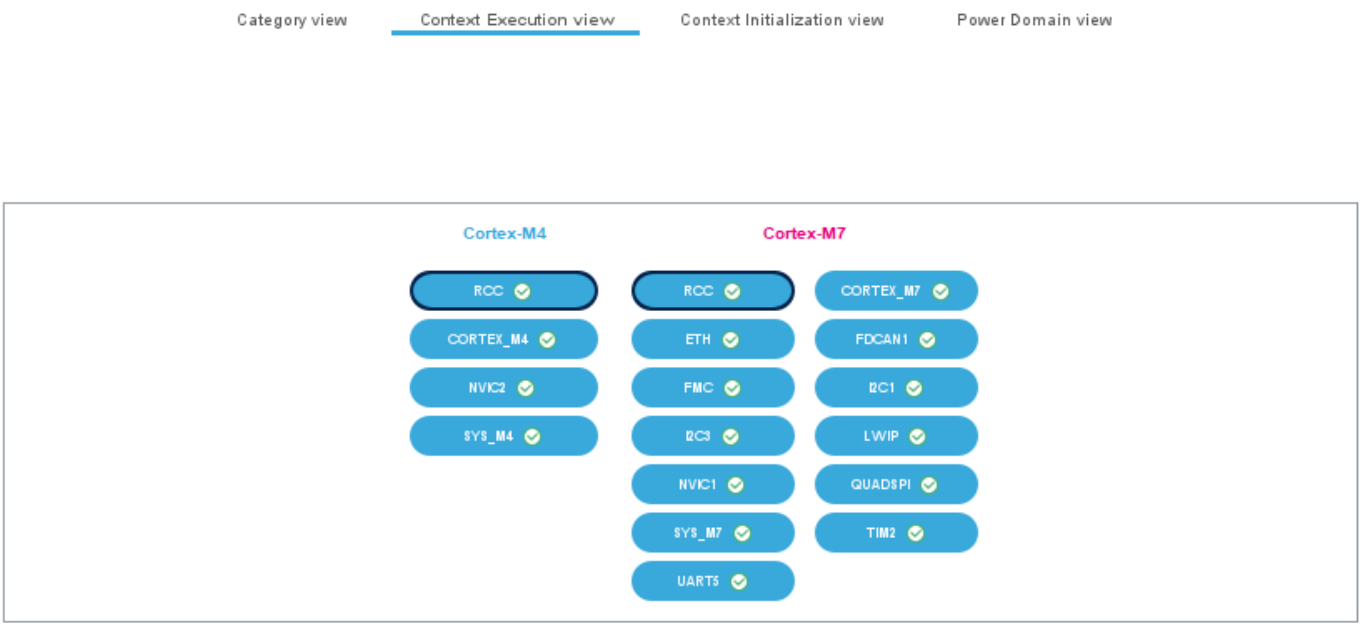
9.1.1. Current



9.1.2. Without filters



9.2. Context Execution view



9.3. Context Initialization view

9.4. Power Domain view

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00602212.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00176879.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00530531.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337873.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00356635.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00533174.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00597308.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00733995.pdf