
STM32
CubeMX

1. Description

1.1. Project

Project Name	L00575-95_DUT-FW
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	11/30/2023

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H745IITx
MCU Package	LQFP176
MCU Pin number	176

1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4

2. Pinout Configuration

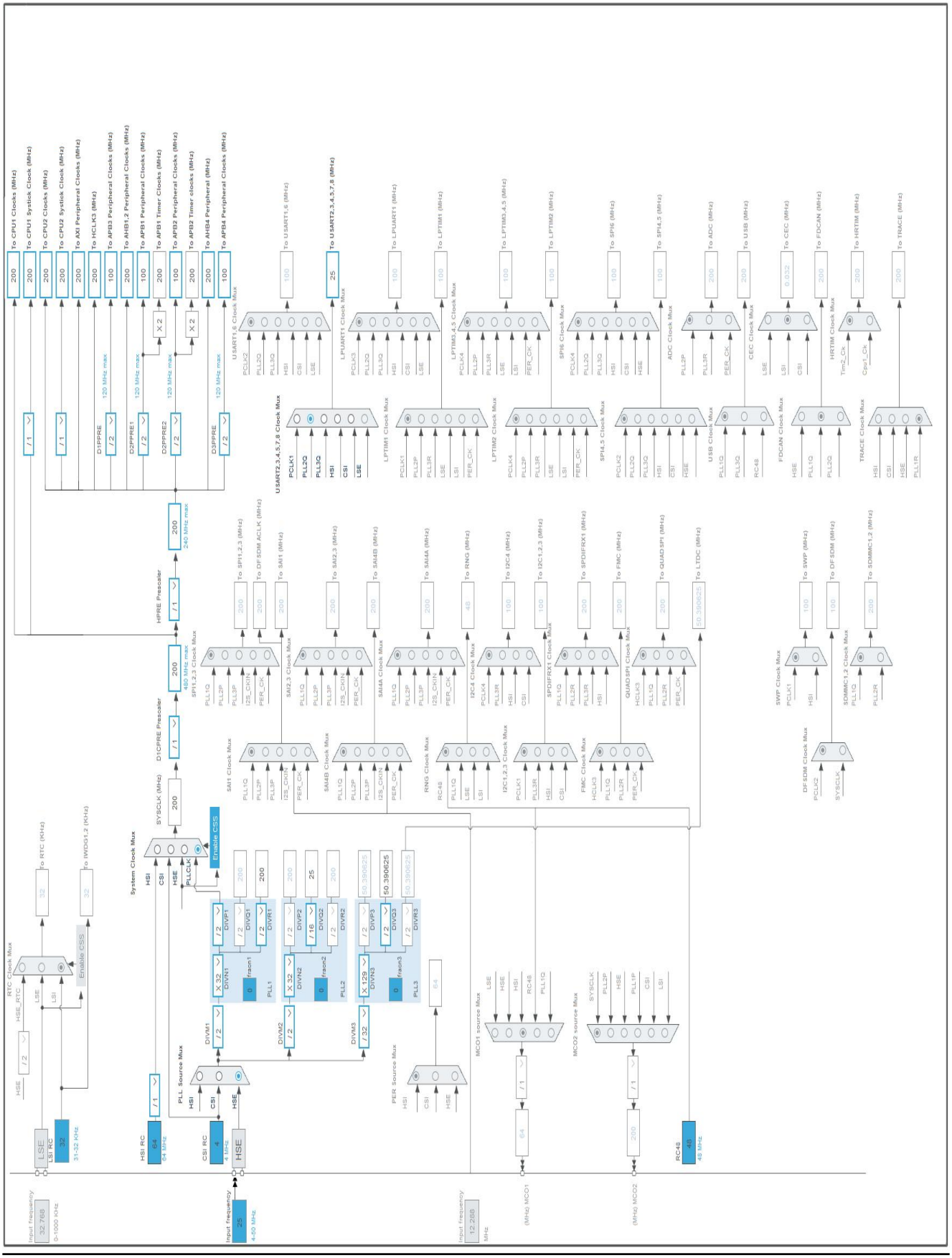
3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VSS	Power		
7	VDD	Power		
8	VBAT	Power		
12	VSS	Power		
13	VDD	Power		
14	VSSSMPS	Power		
15	VLXSMPS	Power		
16	VDDSMPS	Power		
17	VFBSMPS	Power		
20	PF2 *	I/O	GPIO_Output	FRONT_LED_2
21	PF3 *	I/O	GPIO_Output	FRONT_LED_1
24	VSS	Power		
25	VDD	Power		
31	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
33	NRST	Reset		
35	PC1	I/O	ETH_MDC	
38	VSSA	Power		
40	VDDA	Power		
42	PA1	I/O	ETH_REF_CLK	
43	PA2	I/O	ETH_MDIO	
44	VDD	Power		
45	VSS	Power		
47	VSS	Power		
48	VDD	Power		
52	PA7	I/O	ETH_CRS_DV	
53	PC4	I/O	ETH_RXD0	
54	PC5	I/O	ETH_RXD1	
64	VSS	Power		
65	VDD	Power		
70	VSS	Power		
71	VDD	Power		
79	PB11	I/O	ETH_TX_EN	
80	VCAP	Power		
81	VSS	Power		
82	VDDLDO	Power		
83	VSS	Power		

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
84	VDD	Power		
85	PB12	I/O	ETH_TXD0	
86	PB13	I/O	ETH_TXD1	
92	VDD	Power		
93	VSS	Power		
99	VDD	Power		
100	VSS	Power		
105	VDD	Power		
106	VSS	Power		
112	VSS	Power		
113	VDD	Power		
119	VSS	Power		
120	VDD50_USB	Power		
121	VDD33_USB	Power		
126	VDD	Power		
132	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
133	VCAP	Power		
134	VSS	Power		
135	VDDLDO	Power		
136	VDD	Power		
137	VSS	Power		
138	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
140	PC10	I/O	USART3_TX	DEBUG_TX
141	PC11	I/O	USART3_RX	DEBUG_RX
151	VSS	Power		
152	VDD	Power		
159	VSS	Power		
160	VDD	Power		
162	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
167	BOOT0	Boot		
172	VCAP	Power		
173	VSS	Power		
174	PDR_ON	Reset		
175	VDDLDO	Power		
176	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	L00575-95_DUT-FW
Project Folder	C:\Users\massimi\OneDrive - RAIT88 Srl\ACMM - Advanced Chassis Monitoring
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART3_UART_Init	USART3
4	MX_LWIP_Init	LWIP

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H745IITx
Datasheet	DS12923_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

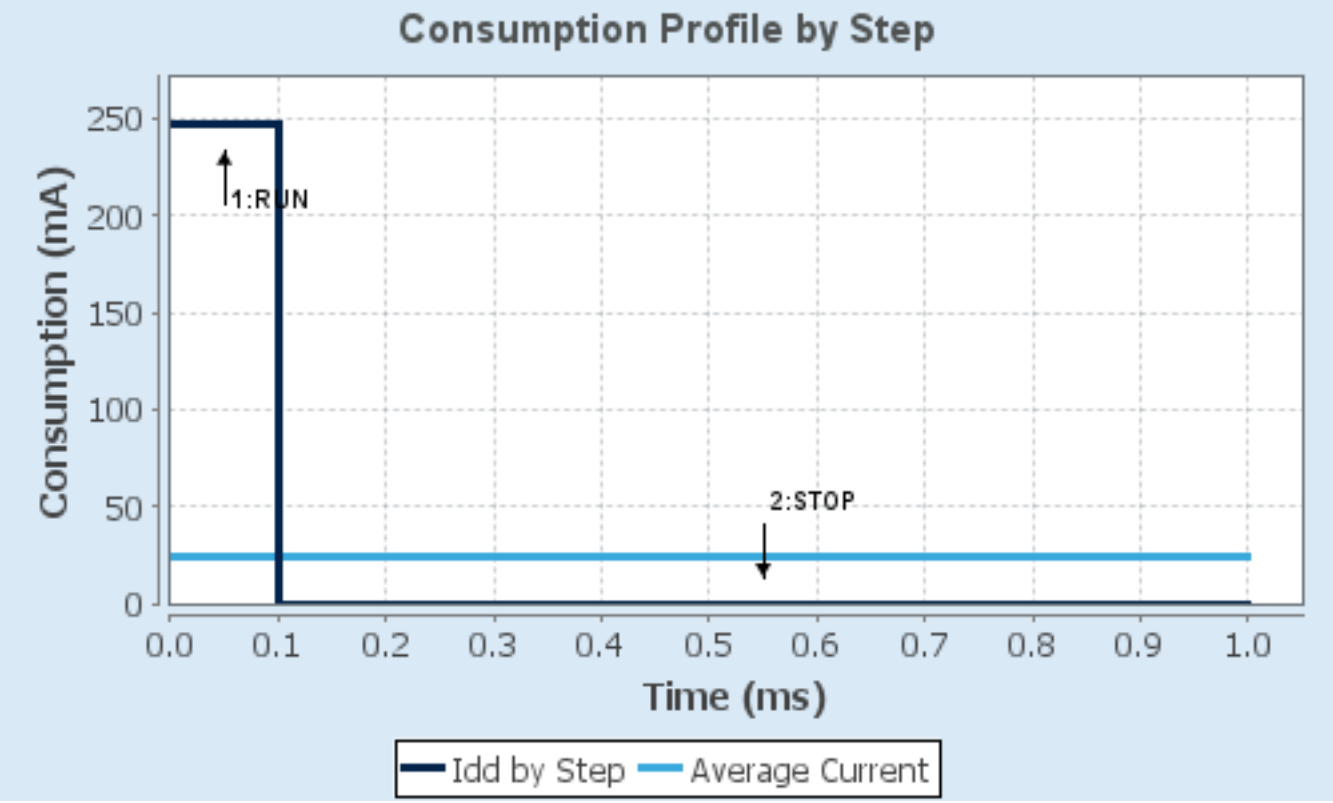
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_IPs_ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
250
200
150
100
50
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. CORTEX_M7

2.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Speculation default mode Settings:

Speculation default mode	Disabled

Cortex Interface Settings:

CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	**Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers ***

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x30000000 ***
MPU Region Size	**32KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	**ENABLE ***
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x30044000 ***
MPU Region Size	**16KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	

	ENABLE *
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

2.2. DEBUG

Debug: Trace Asynchronous Sw

2.2.1. Core(s) Settings:

Context(s):	Cortex-M7

	Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	

2.3. ETH

Mode: RMII

2.3.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30000200 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30000000 ***
Rx Buffers Length	1536

2.4. RCC

High Speed Clock (HSE): BYPASS Clock Source

2.4.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
	Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)
Product revision	rev.V

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

2.5. SYS_M4

Timebase Source: SysTick

2.5.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

2.6. SYS

Timebase Source: SysTick

2.6.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

2.7. USART3

Mode: Asynchronous

2.7.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.8. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

2.8.1. General Settings:

Core(s) Settings:

Context(s):	Cortex-M7

Initialized Context:	Cortex-M7
Power Domain:	D1

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	**Disabled ***

IP Address Settings:

IP_ADDRESS (IP Address)	**010.000.001.100 ***
NETMASK_ADDRESS (Netmask Address)	**255.255.255.000 ***
GATEWAY_ADDRESS (Gateway Address)	**010.000.001.001 ***

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Disabled
RTOS_USE_NEWLIB_REENTRANT (No RTOS - 2)	Disabled

Platform Settings:

PHY Driver	Choose/LAN8742

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

2.8.2. Key Options:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Not Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	**10*1024 ***
LWIP_RAM_HEAP_POINTER (RAM Heap Pointer)	**0x30044000 ***

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Disabled

2.8.3. PPP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

2.8.4. IPv6:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

2.8.5. HTTPD:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

2.8.6. SNMP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

2.8.7. SNTP/SMTP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)	Disabled

2.8.8. MDNS/TFTP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

2.8.9. Perf/Checks:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

2.8.10. Statistics:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

2.8.11. Checksum:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Enabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	**Enabled ***
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Enabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

2.8.12. Debug:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

2.8.13. Platform Settings:

Driver_PHY	LAN8742

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB3 (JTDO/TRACESWO	DEBUG_JTDO-SWO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	DEBUG_TX	Cortex-M7	D2
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	DEBUG_RX	Cortex-M7	D2
GPIO	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FRONT_LED_2	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PF3	GPIO_Output	Output Push Pull	No pull-up and no pull-	Low	FRONT_LED_1	Cortex-M7*	Cortex-M7*

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
				down			Cortex-M4	Cortex-M4

* Initialized context

3.2. DMA configuration

nothing configured in DMA service

3.3. BDMA configuration

nothing configured in DMA service

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART3 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
CM4 send event interrupt for CM7	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

3.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

3.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
CM7 send event interrupt for CM4	unused		
FPU global interrupt	unused		
HSEM2 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

3.5.4. NVIC2 Code generation

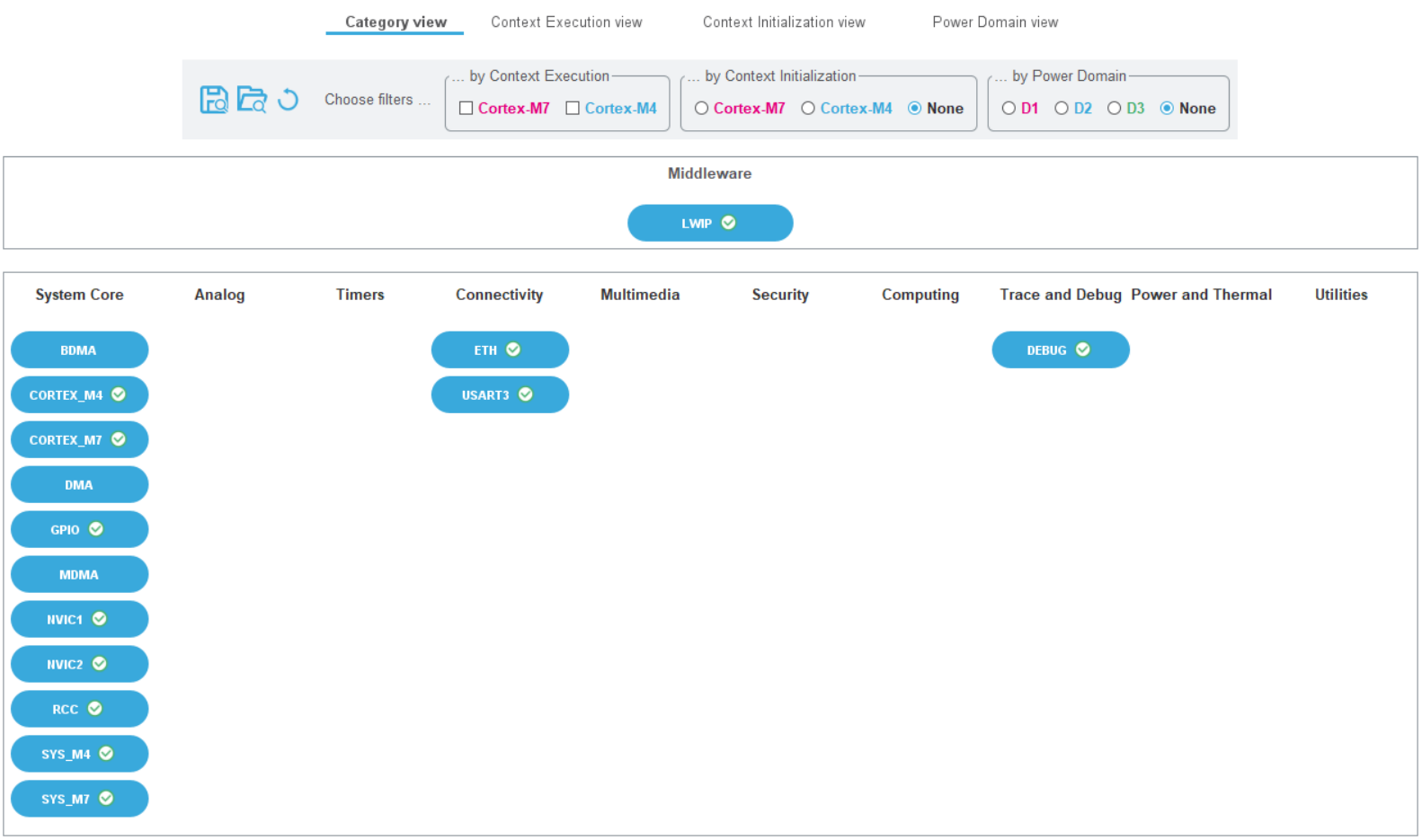
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

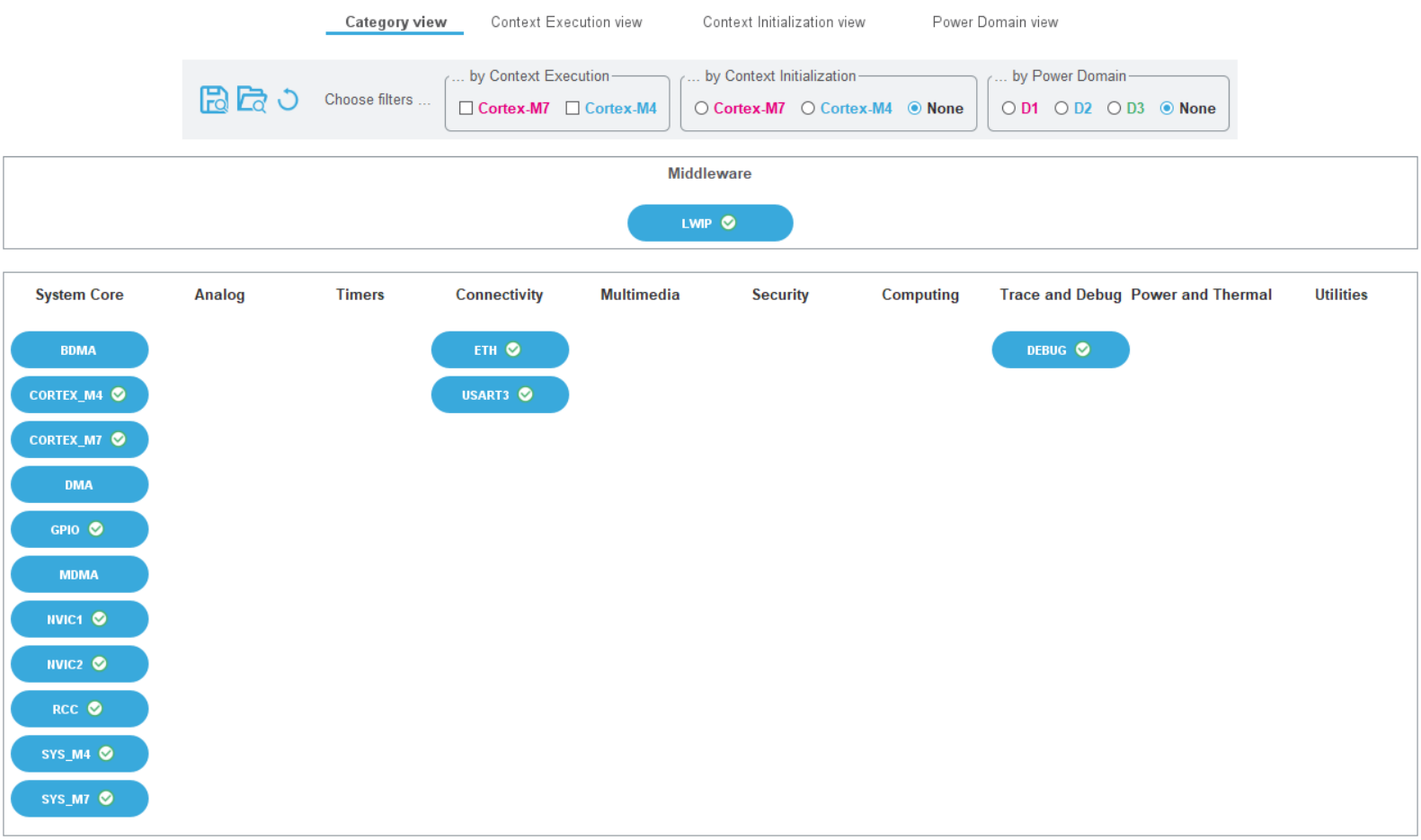
4. System Views

4.1. Category view

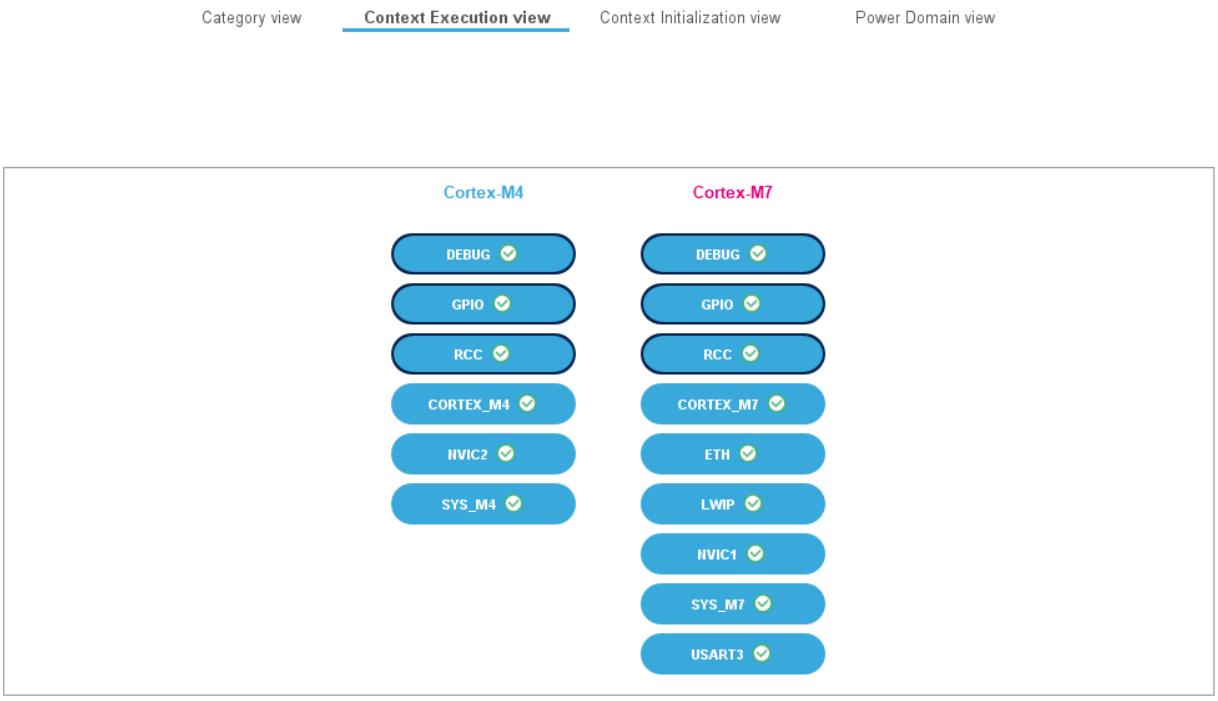
4.1.1. Current



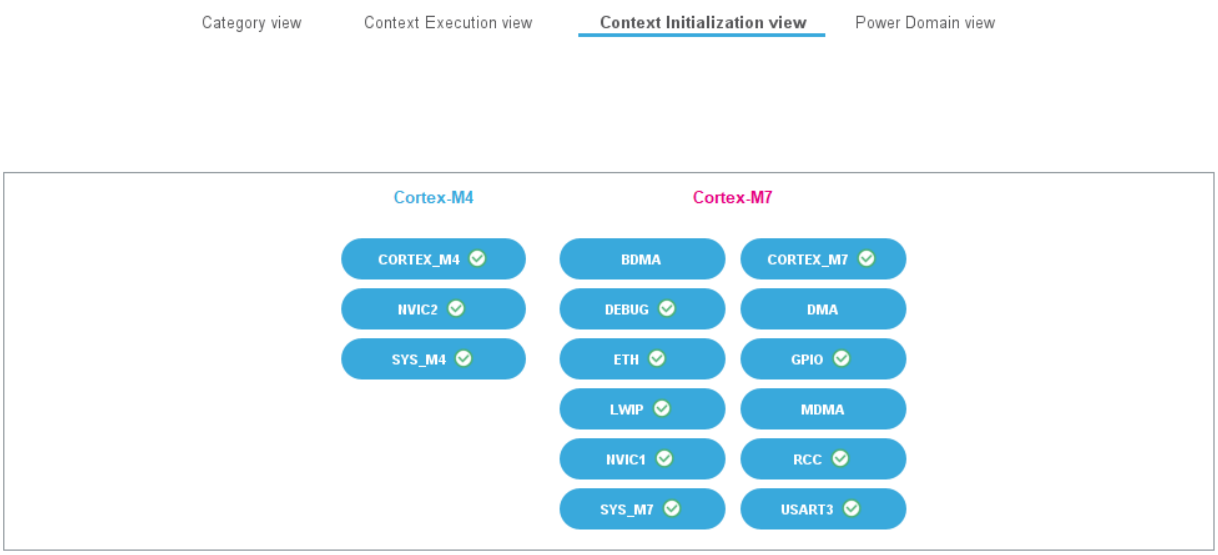
4.1.2. Without filters



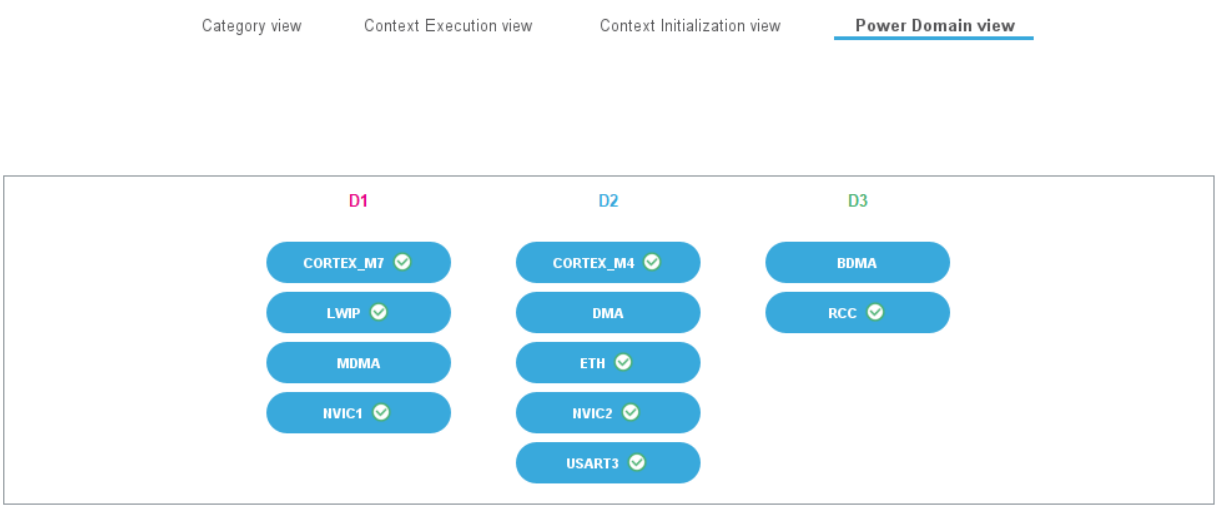
4.2. Context Execution view



4.3. Context Initialization view



4.4. Power Domain view



5. Docs & Resources

Type	Link