STM32 Updates for technical development community

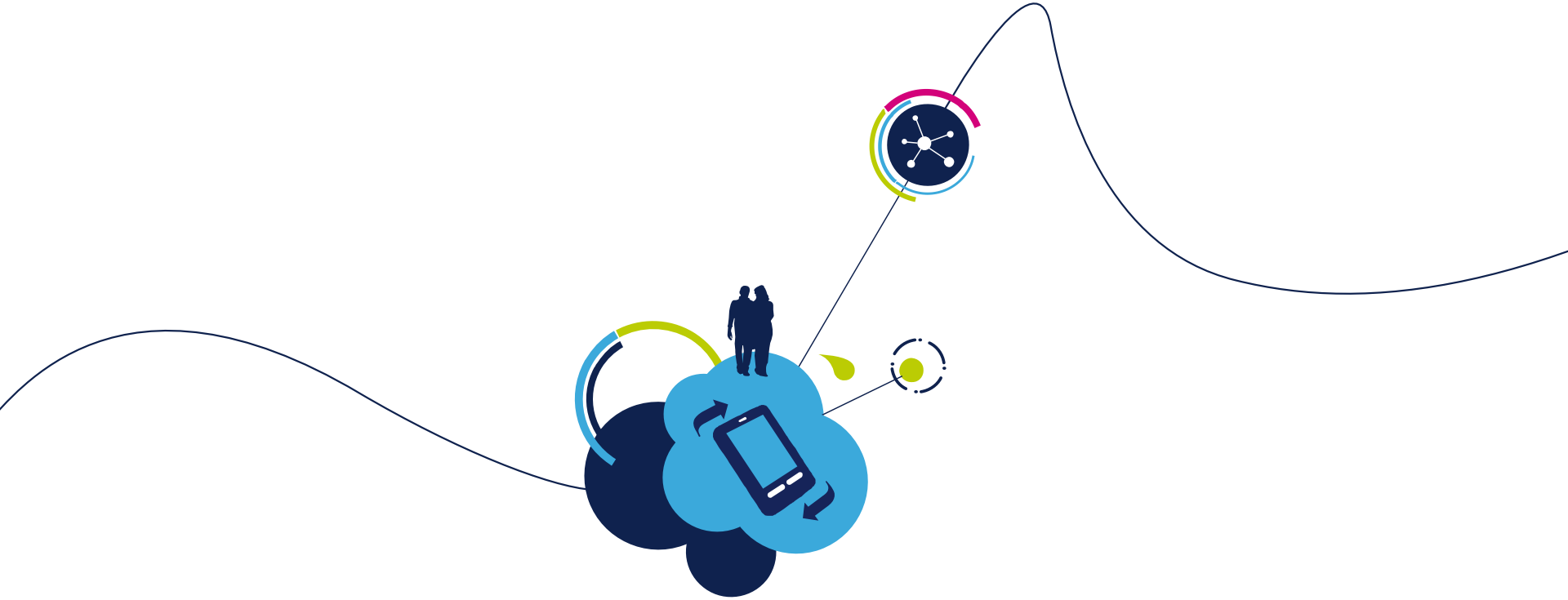
Microcontrollers Division

2012 – 1st Issue

life.augmented

Contents

Contents



Documents Major Updates

Documents Major Updates Overview

- STM32F205x and STM32F207x datasheet Rev8 **(On Web)**
- STM32F215x and STM32F217x datasheet Rev6 **(On Web)**
- STM32F40xx and STM32F41xx datasheet Rev2 **(On Web)**
- STM32F103xFG datasheet Rev3 **(On Web)**
- STM32F100BDIE STM32 value line die Specification Rev2 **(On Web)**
- STM32F20x and STM32F21x Errata sheet - Rev2 **(On Web)**
  STM32F40x STM32F41x Errata sheet - Rev2 **(On Web)**
  STM32F105/107xx Errata sheet - Rev8 **(On Web)**
- AN2606 “STM32 microcontroller system memory boot mode” Rev13
  AN2586 “STM32F10xxx hardware getting started” Rev7 **(On Web)**

STM32 Documents Major Updates (1/11)

- STM32F20xx Datasheet Rev8
  STM32F21xx Datasheet Rev6 **(On Web)**
  - Add FSMC, SDIO, ULPI , Ethernet MII and RMII setup/hold timings
  - OTG_FS external PHY was removed.
    - OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions removed.
  - NEW: Added maximum power consumption at TA=25 °C for STOP mode.

Table 20. Typical and maximum current consumptions in Stop mode(1)

Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00	
	Supply current in Stop mode with main regulator in Low Power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00	

STM32 Documents Major Updates (2/11)

- STM32F4xxx Datasheet Rev2 **(On Web)**
  - Add New WLCSP90 Package (Pinout will be described in Rev3)
  - New pins table definitions:

Table 6. STM32F41x pin and ball definitions

Pin number					Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176						
-	1	1	A2	1	PE2	I/O	FT		TRACECLK/ FSMC_A23 / ETH_MII_TXD3 / EVENTOUT	
-	2	2	A1	2	PE3	I/O	FT		TRACED0/FSMC_A19 / EVENTOUT	

  - "Notes" column : handle special pins and exceptions
  - Differentiate
    - Alternate functions: Functions selected through GPIOx_AFR registers
    - Additional functions : Functions directly selected/enabled through peripheral registers

STM32 Documents Major Updates (3/11)

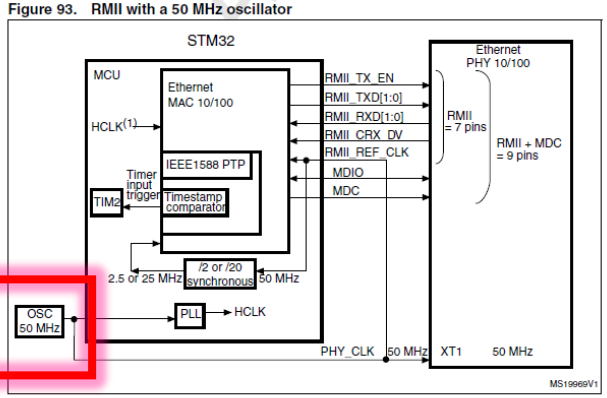
- STM32F4xxx Datasheet Rev2 **(On Web)**
  - Some important Highlights in datasheet versus F2 series
    - Table 12 : Limitations depending on the operating power supply range
      - Prefetch is not available for VDD=1.8 to 2.1Volt range Refer to AN3430 application note for details on how to adjust performance and power.
    - HSE in bypass mode can have an external Frequency up to 50MHz instead of 26MHz

Table 26. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)		1	8	50	MHz

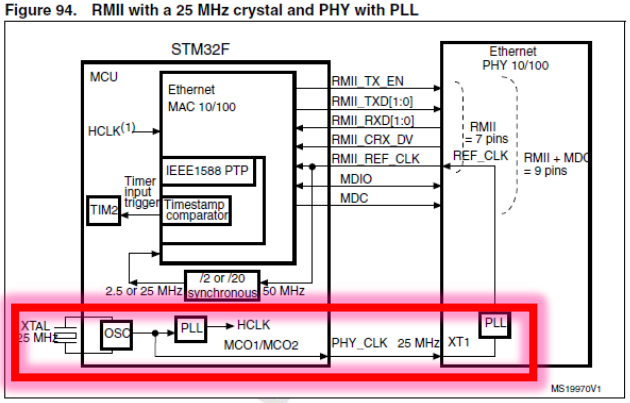
- Ethernet Interface with External PHY for RMII mode

Figure 93. RMII with a 50 MHz oscillator



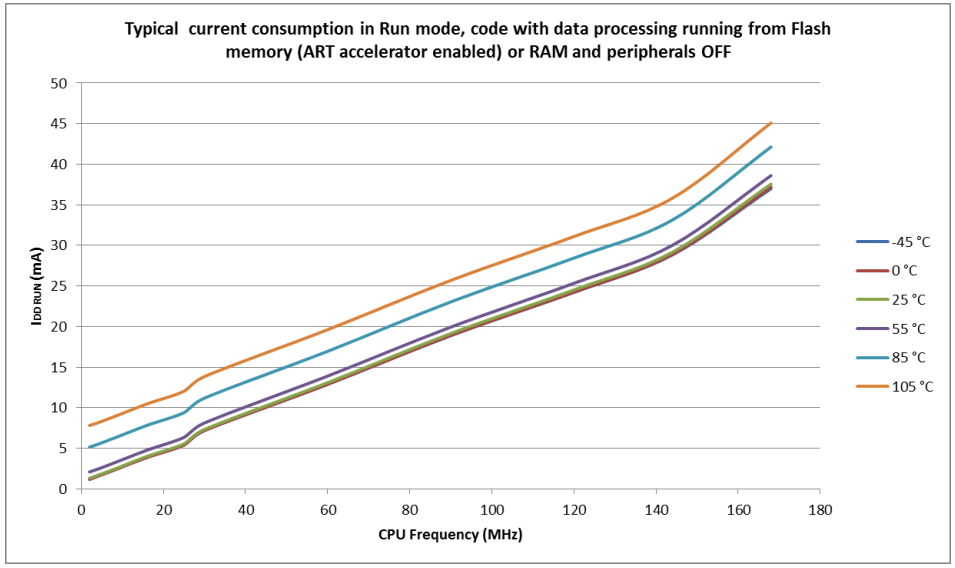
1. f_{HCLK} must be greater than 25 MHz.

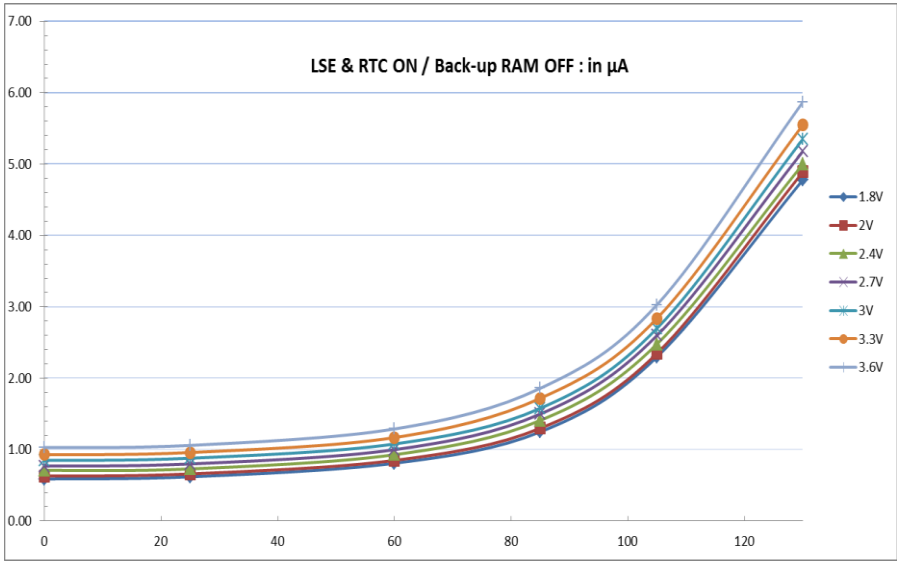
Figure 94. RMII with a 25 MHz crystal and PHY with PLL



STM32 Documents Major Updates (4/11)

- STM32F4xxx Datasheet Rev2 **(On Web)**
  - Most of Parametrics are now available
    - Typical and maximum current consumption in RUN/Sleep, STOP, Standby and VBAT modes
      - Exception with Max in Standby and VBAT mode when RTC and LSE is ON, still TBD, but new curves added for temperature variation on typical devices





STM32 Documents Major Updates (5/11)

- STM32F4xxx Datasheet Rev2 **(On Web)**
  - Most of Parametric are now available
    - New section added “I/O dynamic current consumption”, When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

I = VDD* Fsw* C

Where

- **I** is the current sunk by a switching I/O to charge/discharge the capacitive load
- **VDD** is the MCU supply voltage
- **F_{SW}** is the I/O switching frequency
- **C** is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency

Table 23. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
I_{DDIO}	I/O switching current	V_{DD} = 3.3 V(2) C = C_{INT}	2 MHz	0.02	mA
			8 MHz	0.14	
			25 MHz	0.51	
			50 MHz	0.86	
			60 MHz	1.30	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.10	
			8 MHz	0.38	
			25 MHz	1.18	
			50 MHz	2.47	
			60 MHz	2.86	
		V_{DD} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.17	
			8 MHz	0.66	
			25 MHz	1.70	
			50 MHz	2.65	
			60 MHz	3.48	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.23	
			8 MHz	0.95	
			25 MHz	3.20	
			50 MHz	4.69	
			60 MHz	8.06	

STM32 Documents Major Updates (6/11)

- STM32F4xxx Datasheet Rev2 **(On Web)**
  - Most of Parametrics are now available
    - Typical Peripherals Current consumption at 168MHz and 144MHz are added (AHB1,AHB2, AHB3, APB1 and APB2).
    - Analog Parametric :
      - ADC : Frequency up to 36MHz, but characterization is done and provided only for 30MHz as F2. still on-going to get new data.
    - Digital Parametric:
      - USB ULPI : added
      - Ethernet RMII : added
      - FSMC : added
      - SPI/I2S/SDIO and Ethernet MII/SMI are planned for Rev3

STM32 Documents Major Updates (7/11)

- STM32F103xFG Datasheet Rev3 **(On Web)**
  - Added FSMC and SDIO timings characterization
- STM32F105/7xx Errata sheet Rev8 **(On Web)**
  - Bootloader limitations moved to AN2606 in “Bootloader version” section
- AN2586 “STM32F10xxx hardware getting started” Rev7 **(On Web)**
  - Added support of STM32F103xFG devices

STM32 Documents Major Updates (8/11)

- AN2606 “STM32 microcontroller system memory boot mode” Rev13
  - Add support for STM32F100xxx and STM32F4xxx devices
  - New bootloader limitation added in “Bootloader version” section for bootloader V2.0
  - New bootloader version V2.1 is available

  - Title : PA9 excessive power consumption when **USB** cable is plugged in bootloader **V2.0**
  - Description
    - When connecting an USB cable after booting from System-Memory mode, PA9 pin (connected to VBUS=5 V) is also shared with USART TX pin which is configured as alternate push-pull and forced to 0 since the USART peripheral is not yet clocked.
    - As a consequence, a current higher than 25 mA is drained by PA9 I/O and may affect the I/O pad reliability.
  - Workaround
    - None.
  - Limitation fixed in **STM32F105xx/107xx bootloader V2.1**. A PIL was sent to our customers

STM32 Documents Major Updates (9/11)

- STM32F20x and STM32F21x Errata sheet Rev2 **(on web)**
  - Title : ART Accelerator prefetch queue instruction is not supported
  - Description
    - The ART Accelerator prefetch queue instruction is not supported when VDD is lower than 2.1V. This limitation does not prevent the ART Accelerator from using the cache enable/disable capability and the selection of the number of wait states according to the system frequency.
  - Workaround
    - None. Refer to application note **AN3430** for details on how to adjust performance and power consumption.

STM32 Documents Major Updates (10/11)

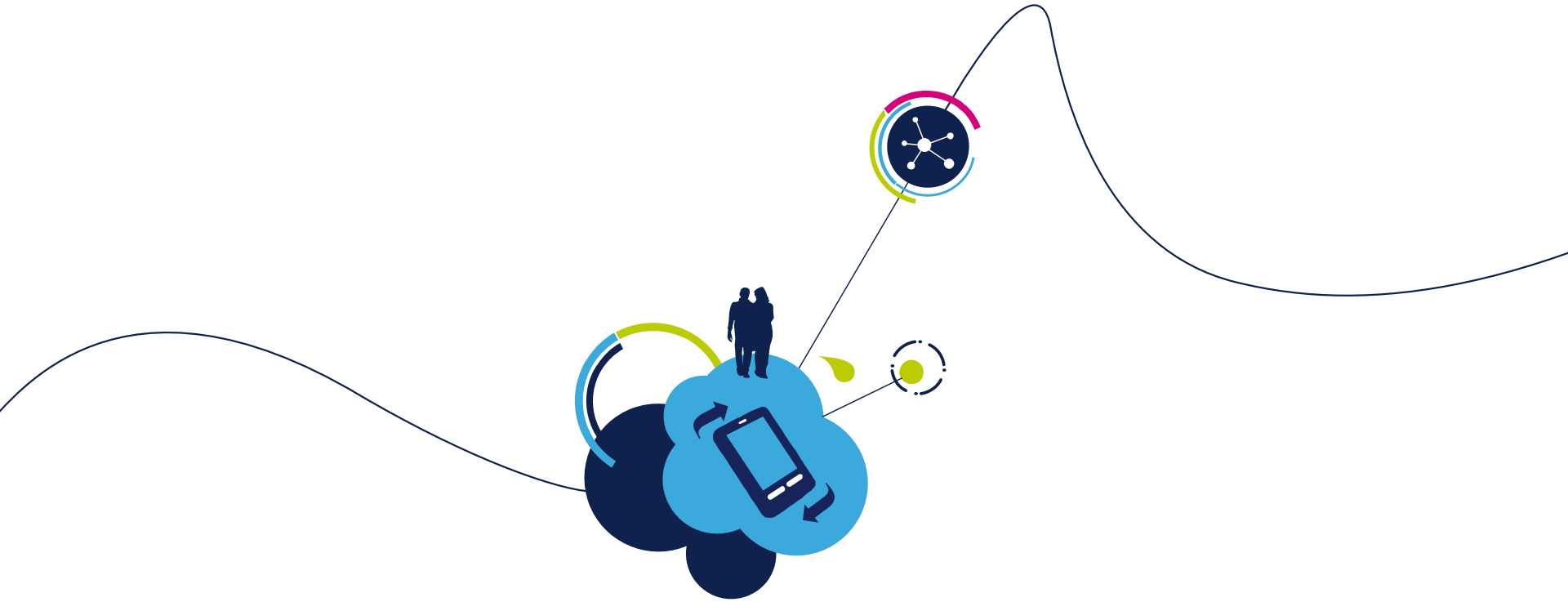
- STM32F40x STM32F41x Errata sheet Rev2 **(on web)**
  - Title : ART Accelerator prefetch queue instruction is not supported
  - Description
    - The ART Accelerator prefetch queue instruction is not supported on revision A devices. This limitation does not prevent the ART Accelerator from using the cache enable/disable capability and the selection of the number of wait states according to the system frequency..
  - Workaround :
    - Revision A devices: None
    - Revision Z devices: Fixed.

STM32 Documents Major Updates (11/11)

- STM32F20x and STM32F21x Errata sheet Rev2 **(on web)**
  STM32F40x STM32F41x Errata sheet Rev2 **(on web)**

  - Title : Configuration of PH10 and PI10 as external interrupts is erroneous
  - Description :
    - PH10 or PI10 are selected as source for EXTI10 external interrupt by setting bits EXTI10[3:0] of SYSCFG_EXTICR3 register to 0x0111 or 0x1000, respectively. However, this operation erroneous enables PH2 and PI2 as external interrupt inputs.
    - As a result, it is not possible to use PH10/PI10 as interrupt sources if PH2/PI2 are not selected as interrupt source. as well. This means that bits **EXTI10[3:0] of SYSCFG_EXTICR3** register and bits **EXTI2[3:0] of SYSCFG_EXTICR1** should be programmed to the same value:
      - 0x0111 to select PH10/PH2
      - 0x1000 to select PI10/PI2
  - Workaround
    - None.

Contents



AN4044 : STM32F4 FPU Application Note and Demo

FPU usage

High level approach
Matrix, mathematical equations

Meta language tools
Matlab ,Scilab…etc…

C code generation
Floating point numbers (`float`)

FPU
Direct mapping
No code modification
High performance
Optimal code efficiency

No FPU
Usage of SW lib
No code modification
Low performance
Medium code efficiency

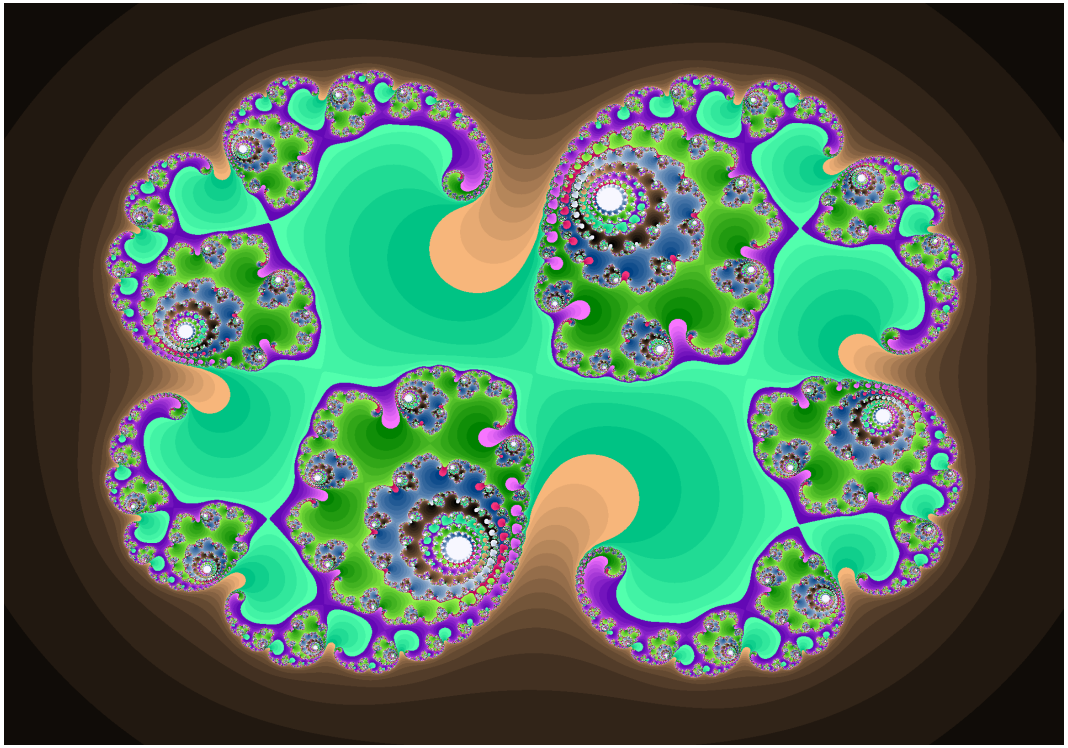
No FPU
Usage of integer based format
Code modification
Corner case behavior to be checked (saturation, scaling)
Medium/high performance
Medium code efficiency

Overview

- The demonstration shows the benefit of FPU on a simple algorithm computing the **Julia set fractal**
- It consists in computing a mathematical sequence for each point of the complex plan and show the speed of divergence for each point
- The mathematical sequence is a complex square elevation with the addition of a constant

Graphical results

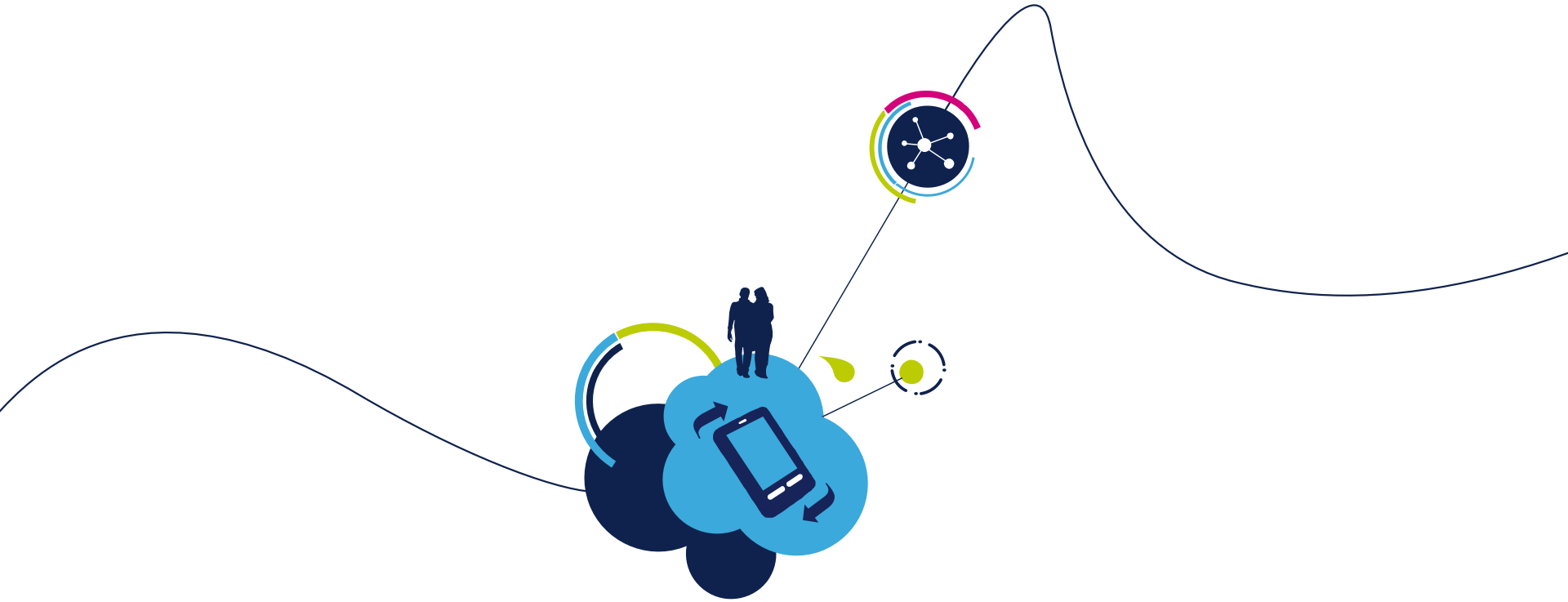
- Associating a color with the divergence speed creates some very nice graphics we all know



FPU efficiency

- The FPU permits a **x11.5 acceleration** for a complete image calculation
- The calculation takes for the complete image **222ms with** the FPU used and **2.597s without** !
- Any application using floats can benefit of such an acceleration (audio decoding/processing, loop control, digital filtering…etc….)

Measures done with MDK-ARM (4.22a) toolchain
Level 3(-O3) for time optimization without MicroLib



AN4004: Using STM32F2 & STM32F4 in DSP applications

life.augmented

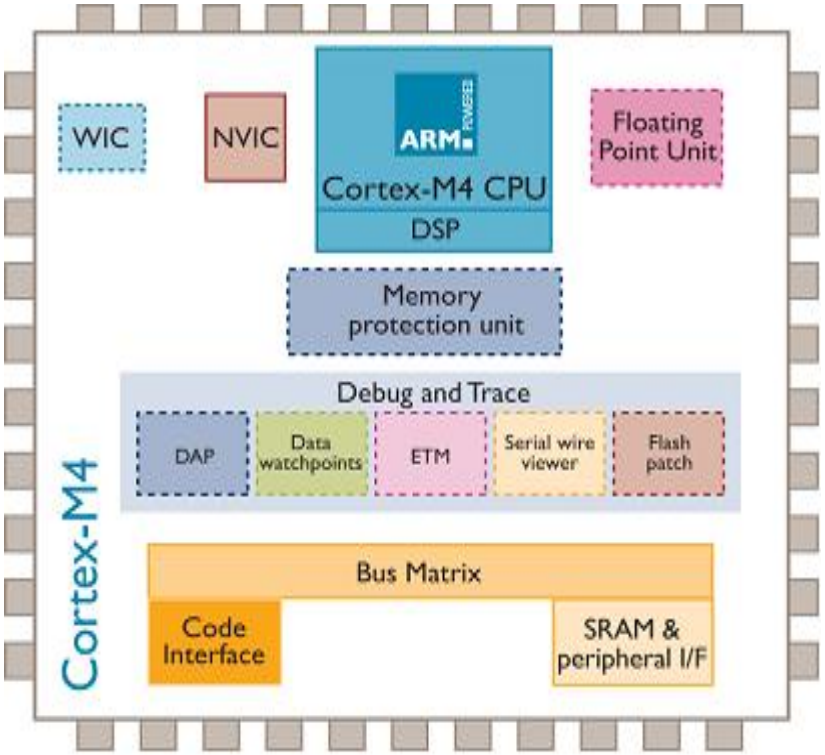
AN4004 Scope & Overview

- This application note (To be published on web : June 2012) describes how to take advantage of the new ARM DSP CMSIS library & use it with STM32F2 or STM32F4. It provides a firmware implementing **FIR** (Finite impulse response) filtering and **FFT** (Fast Fourier transform) as DSP examples with Fixed & Floating point data as input.

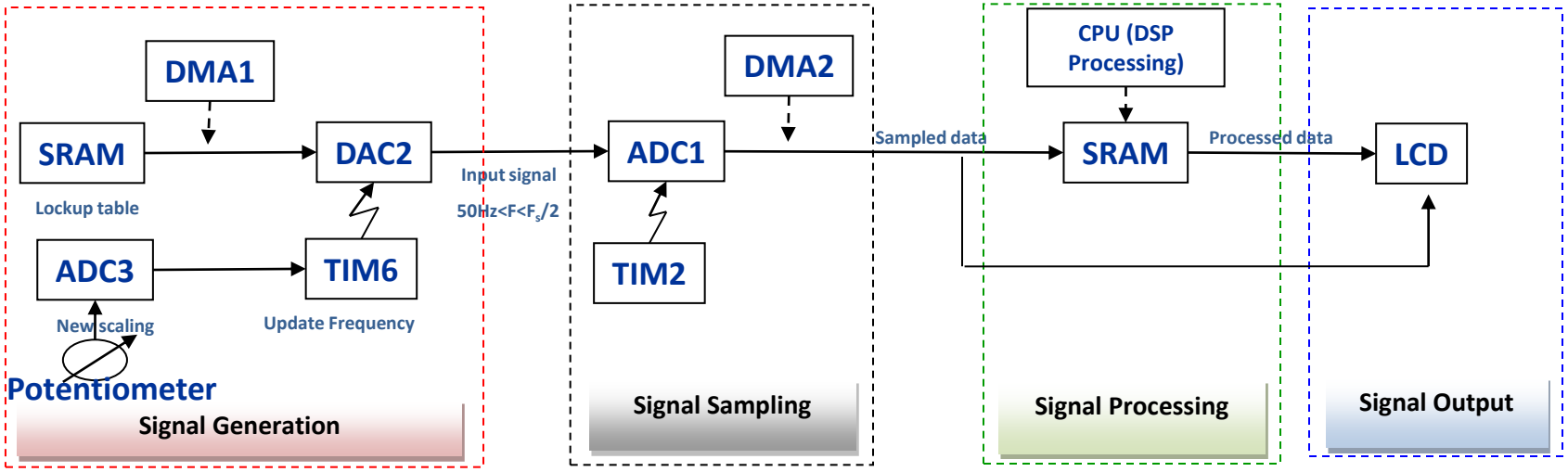
- The following items are described in this AN
  - Overview of main features of STM32F4xx compared to STM32F2xx
  - Cortex-M4F Architecture & main features
  - Overview of the CMSIS DSP library
  - FIR & FFT Examples
    - A small description
    - The hardware setup
    - The firmware architecture
    - The benchmarking results

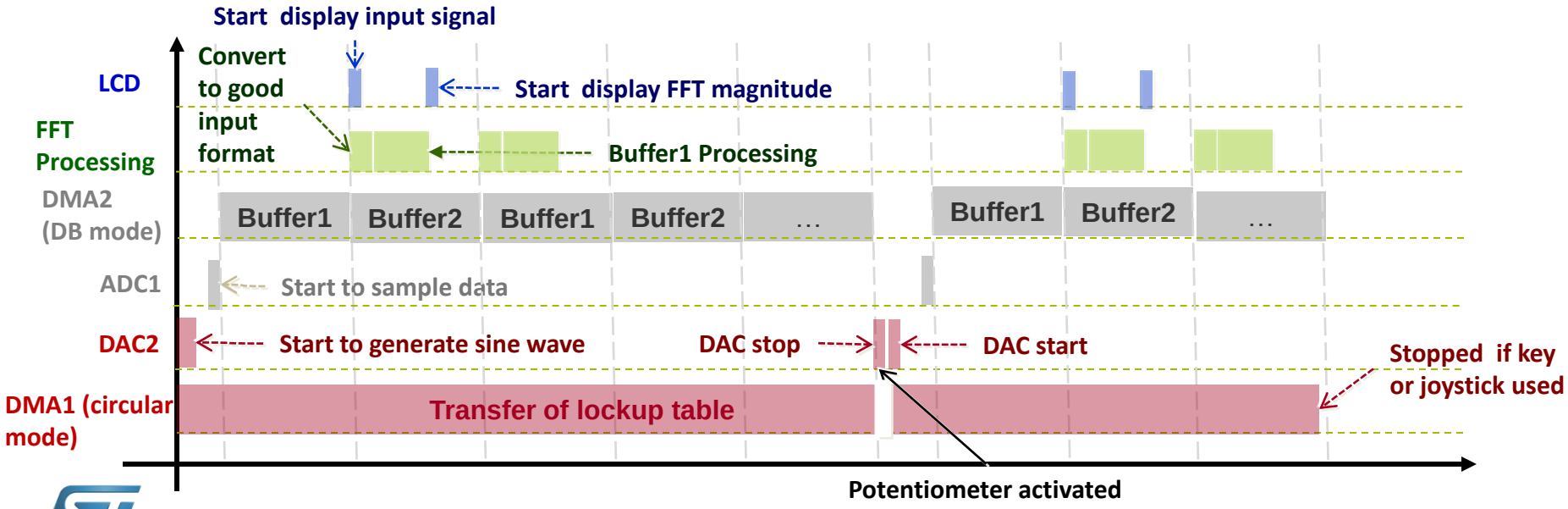
Cortex-M4F main features

- FPU
- Single-cycle SIMD instructions
- Saturated arithmetic
- Barrel shifter
- 8-bit & 16-bit packed data types

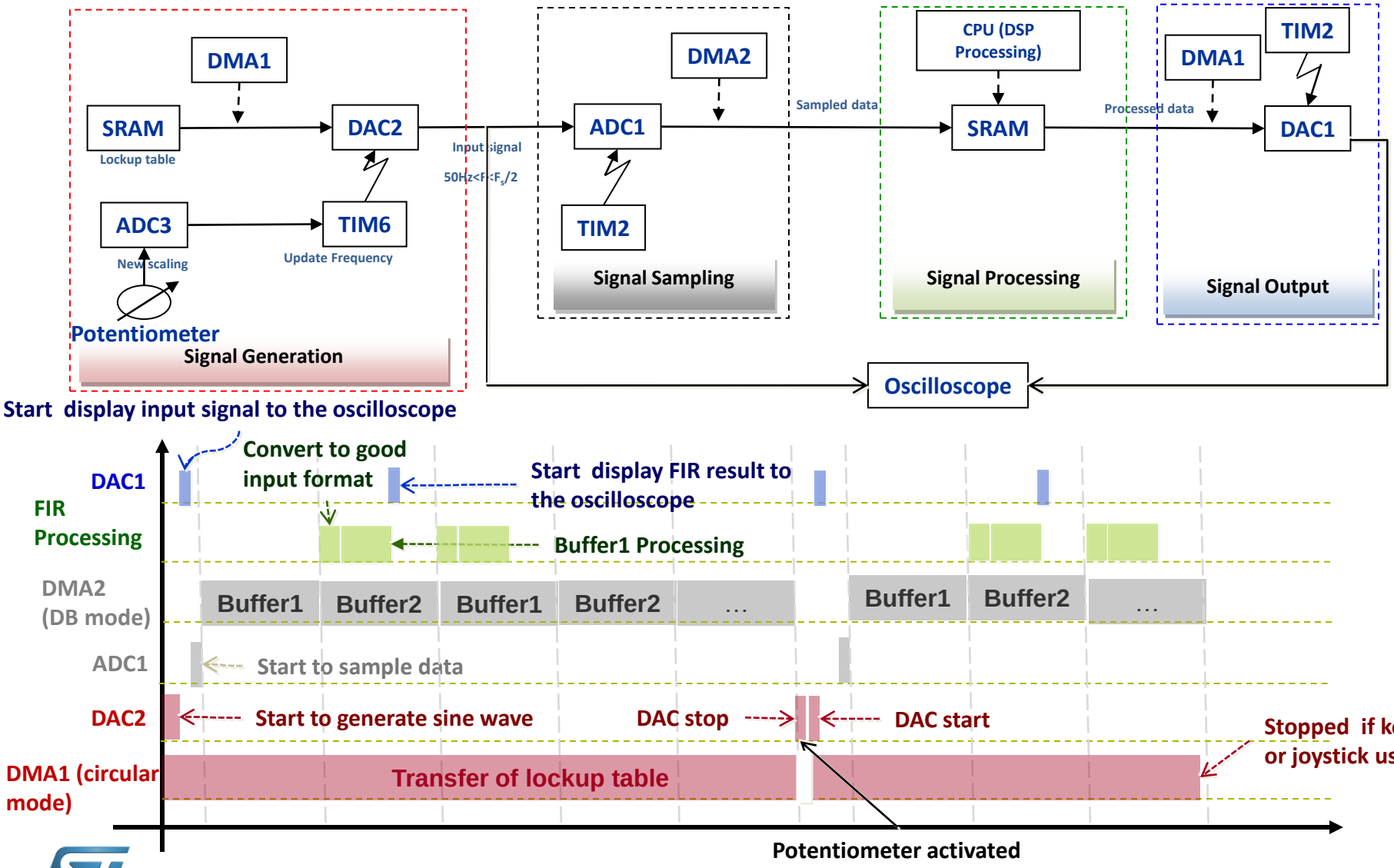


FFT: Hardware setup & data flow

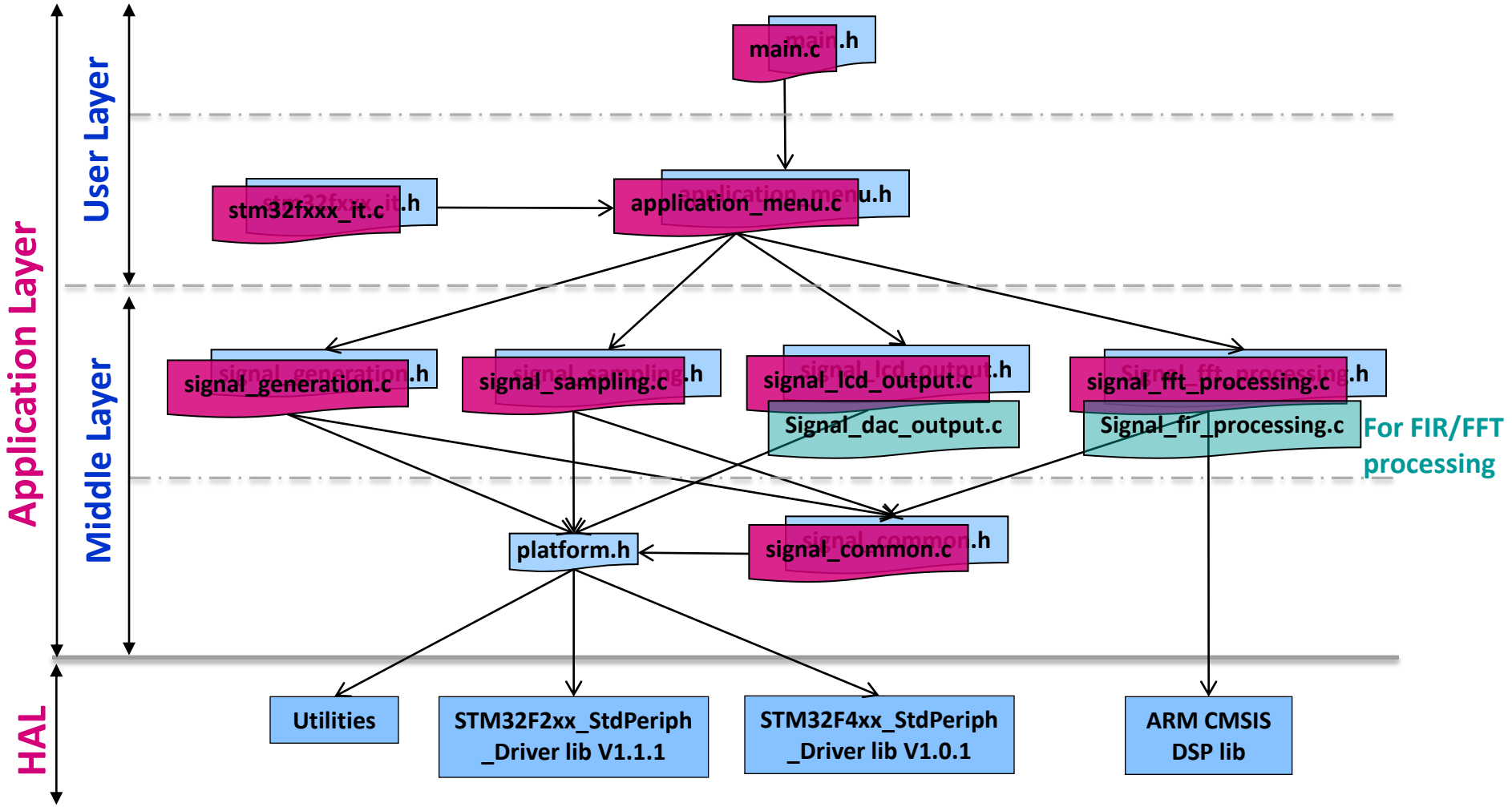




FIR: Hardware setup & data flow



Firmware architecture

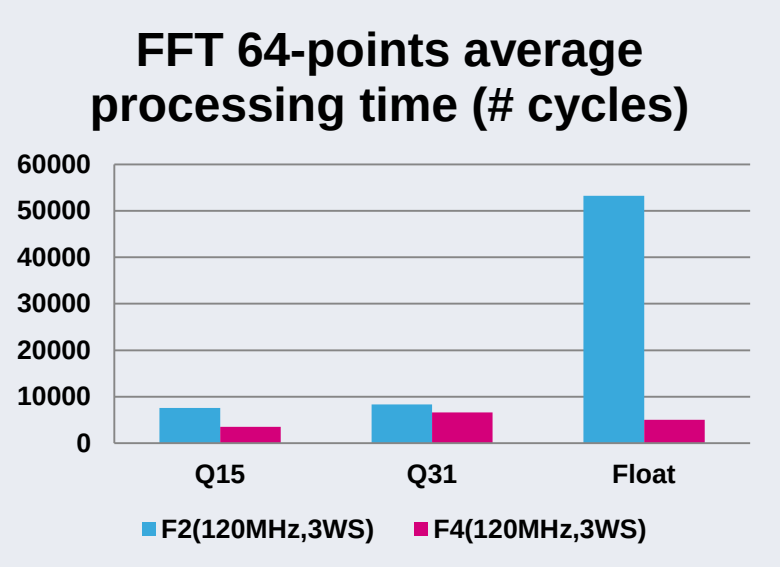


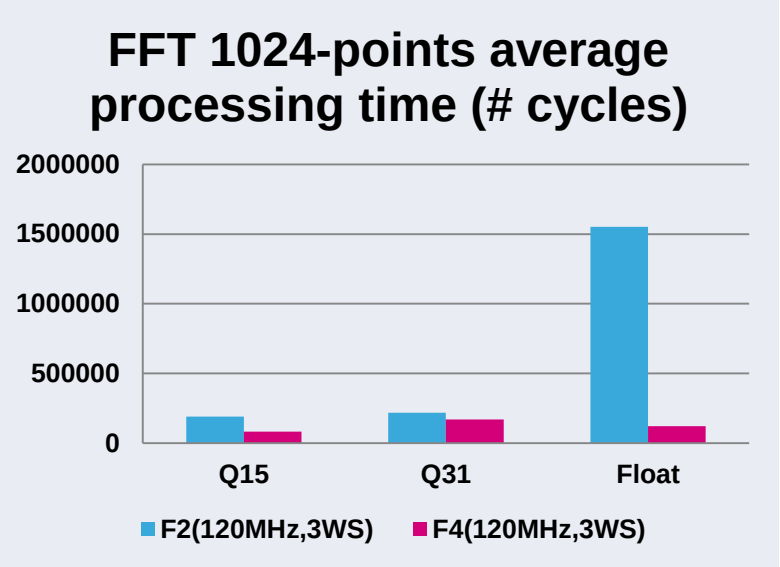
FFT Benchmarking results Setup

Input signal characteristics	
Input signal	a sine wave with a frequency F 50Hz <F<4KHz
Sampling frequency	8KHz

Measures done with MDK-ARM (4.23.00.0) toolchain
Level 3(-O3) for time optimization without MicroLib

FFT Benchmarking results Cortex-M3 vs Cortex-M4F



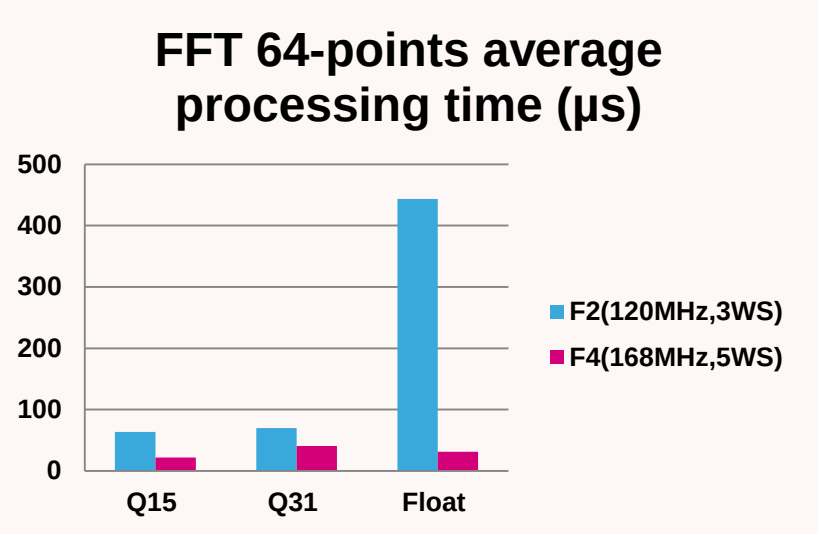


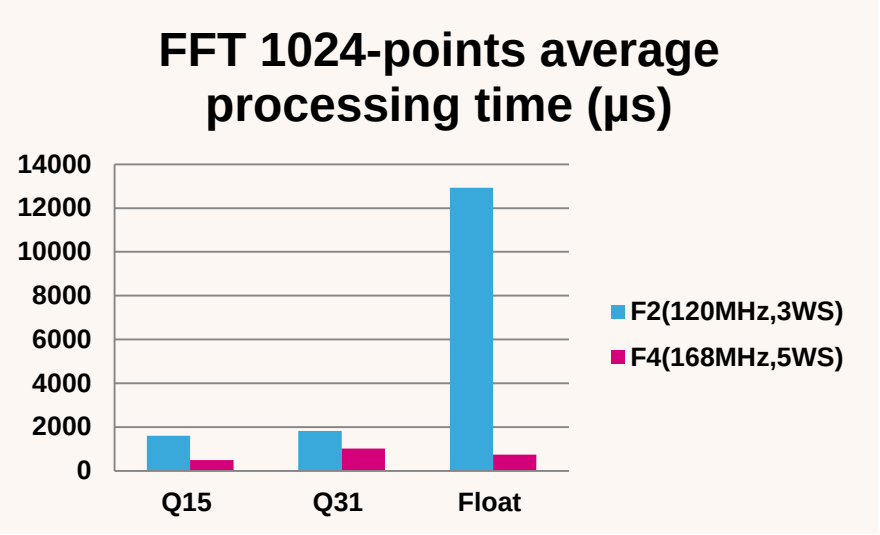
		F2(120MHz,3WS) (#cycles)	F4(120MHz,3WS) (#cycles)	Gain
FFT (64-points)	Q15	7613	3537	x 2.15
	Q31	8362	6656	x 1.25
	Float	53233	5038	x 10
FFT (1024-points)	Q15	192008	82174	x 2.33
	Q31	219077	169484	x 1.3
	Float	1550715	121801	x 12

F2: SW Floating Point

F4: HW FPU used

FFT Benchmarking results F2 vs F4





		F2(120MHz,3WS) (µs)	F4(168MHz,5WS) (µs)	Gain
FFT (64-points)	Q15	63.442	22.101	x 2.9
	Q31	69.683	40.679	x 1.7
	Float	443.608	30.988	x 14.3
FFT (1024-points)	Q15	1600.067	496.952	x 3.22
	Q31	1825.642	1021.208	x 1.7
	Float	12922.625	737.333	x 17.5

F2: SW Floating Point

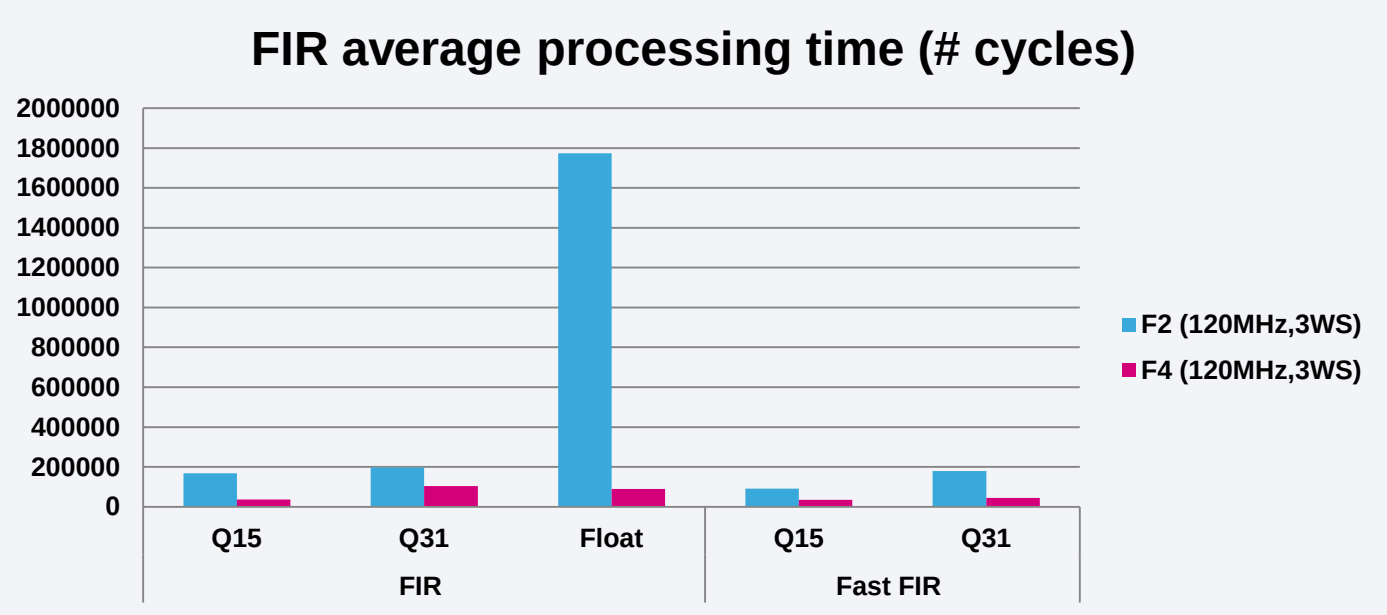
F4: HW FPU used

FIR benchmarking results Setup

Filter & input signal characteristics	
Filter type	Stop Band
Filter order	165
Filter coefficients	166
Cut-off frequency	F_{STOP1}=1.9KHz, F_{STOP2}=2.1KHz
Sampling frequency	48KHz
Number of samples	128
Input signal	a sine wave with a frequency F 50Hz <F<4KHz

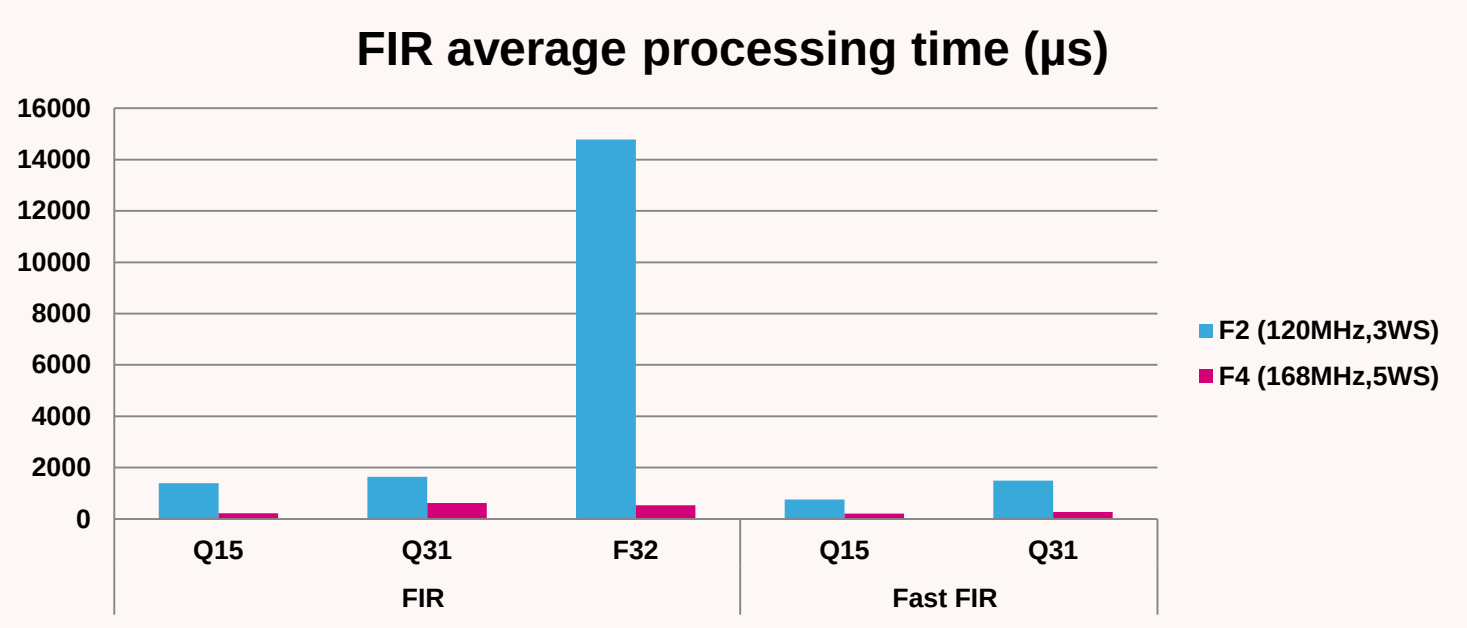
Measures done with MDK-ARM (4.23.00.0) toolchain Level 3(-O3) for time optimization without MicroLib

FIR Benchmarking results Cortex-M3 vs Cortex-M4F



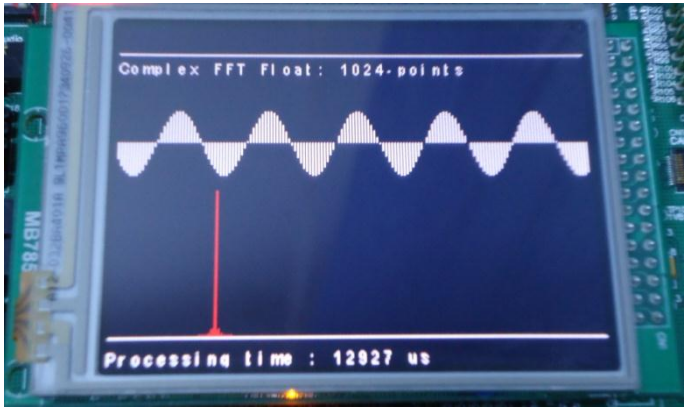
		F2(120MHz,3WS) (#cycles)	F4(120MHz,3WS) (#cycles)	(gain)
FIR	Q15	167639	36620	~ x 4.5
	Q31	196399	104105	~ x 1.9
	Float	1773901	89439	~ x 19
Fast FIR	Q15	91281	35293	~ x 2.5
	Q31	178595	45034	~ x 4

FIR Benchmarking results F2 vs F4



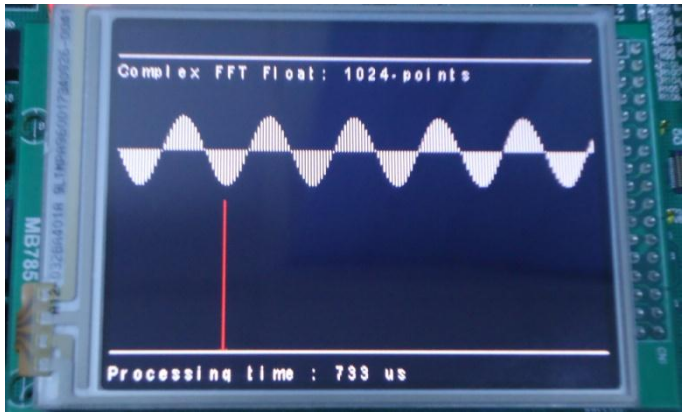
		F2(120MHz,3WS)	Processing time per Tap	F4(168MHz,5WS)	Processing time per Tap
FIR	Q15	1396.992 µs	66ns	218.280 µs	10 ns
	Q31	1636.658 µs	77ns	618.273 µs	29 ns
	Float	14782.510 µs	696ns	531.160 µs	25 ns
Fast FIR	Q15	760.675 µs	36ns	209.761 µs	10 ns
	Q31	1488.292 µs	70ns	267.464 µs	13 ns

Complex FFT-1024 points demos



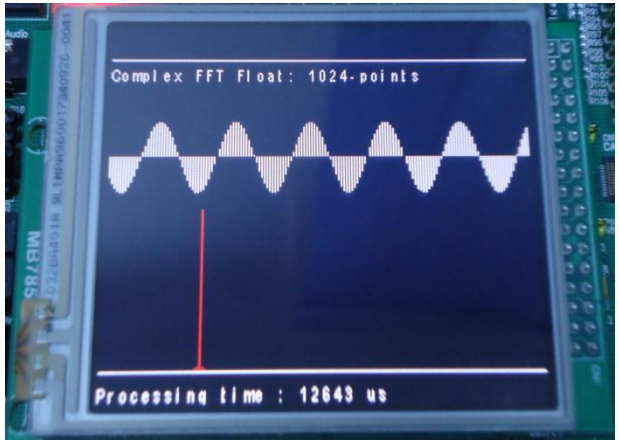
Cortex-M3 running Cortex-M3 code

12927µs

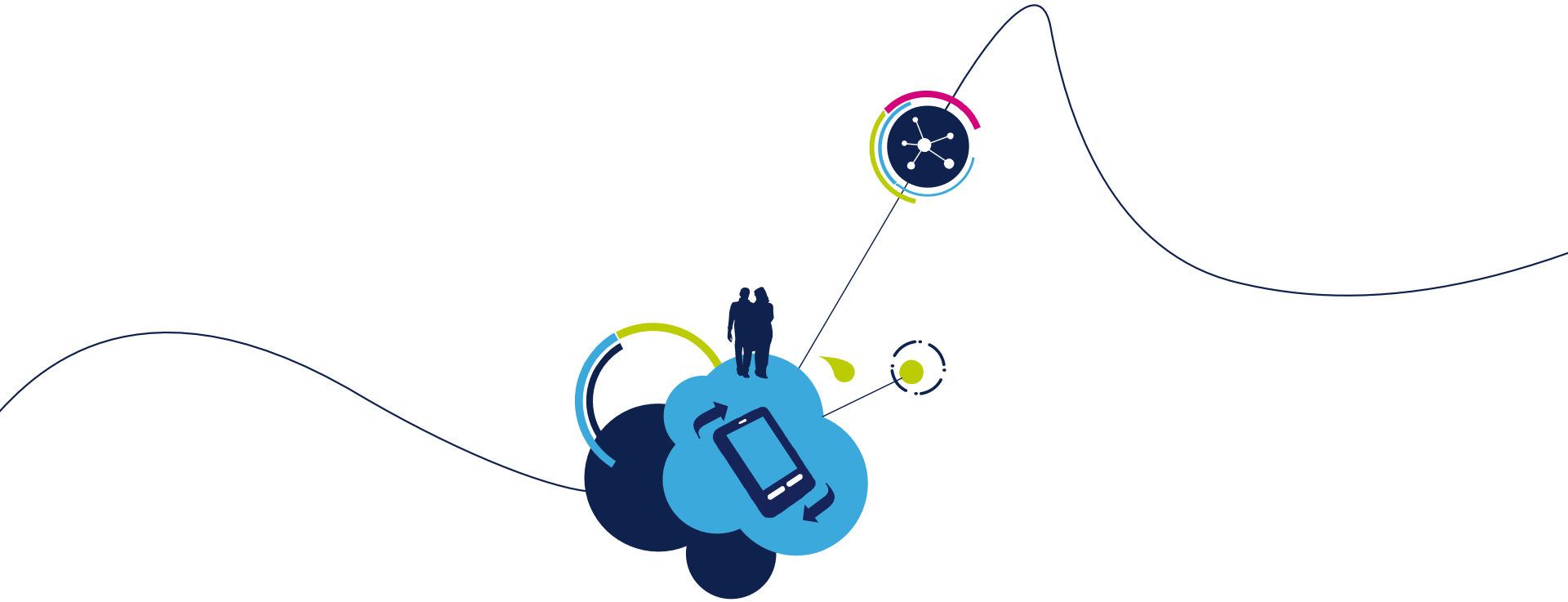


Cortex-M4F running Cortex-M4F code

733µs



Cortex-M4F running Cortex-M3 code 12643µs



STM32F4xx Memories & Bus Matrix

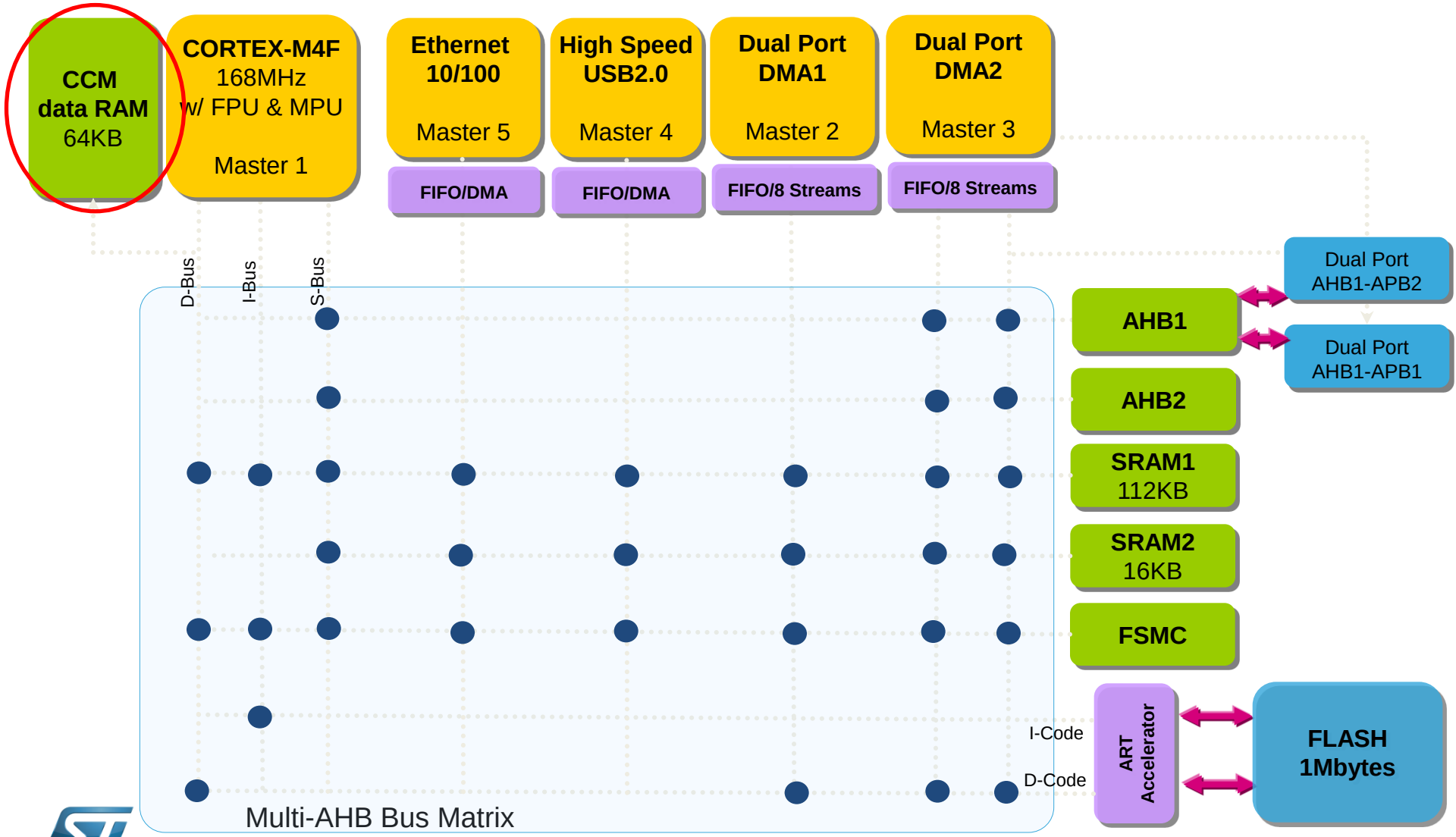
Bus Matrix behavior, CCM and SRAM remap

life.augmented

Scope

- This presentation aims to focus on STM32F4 system architecture, performance of some SRAM remapping configuration and Core Coupled Memory Advantages (CCM on CPU D-Bus).

STM32F4xx system architecture



CCM main advantages (1/2)

- Extends memory capacity with 64KB additional SRAM (Base address: 0x10000000). The CCM address space is not contiguous with main SRAM (SRAM1 & SRAM2).

- Allows to secure application:
  - Kernel (privileged application) Heap and Stack on CCM
  - Application will use SRAM1 & SRAM2

  →Avoid unauthorized accesses :
    - No DMA access is possible,
    - MPU can protect the full CCM memory range from unauthorized accesses.

CCM main advantages (2/2)

- Ensures a good and efficient operation when several peripherals (high-speed peripherals) are working simultaneously :
  - USB HS,
  - Ethernet,
  - Camera interface,
  - FSMC

→Enhance CPU performances by avoiding (concurrency) to access the RAM

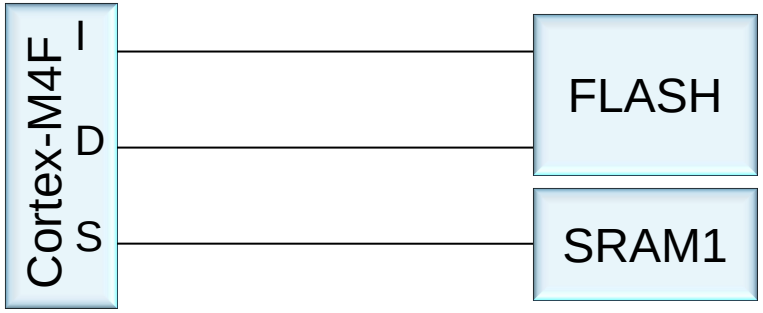
  - In case of many masters requesting access to the SRAM1/2, Bus Matrix apply Round Robin policy to grant accesses.

Performance test example description

- For an example of application using only the memory with no usage of peripherals. Only the CPU is active (no DMAs transfer)
- We can test different system configuration : execution from FLASH, SRAM, remapped SRAM,…
- The test program is counting the number of iterations executed by CPU in a fixed period of time.

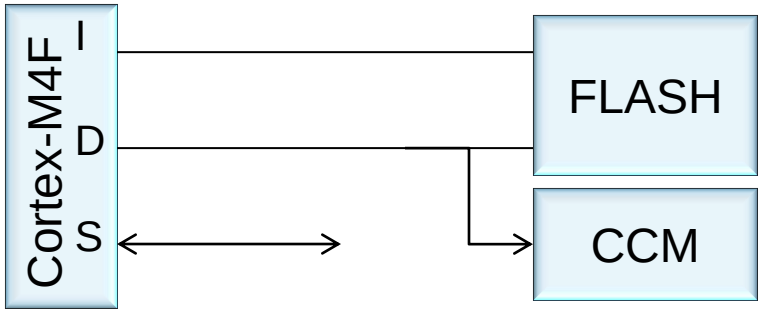
Performance test configuration (1/3)

- Config 1



- In default configuration all accesses are 0-ws, each bus is connected to its default slave.

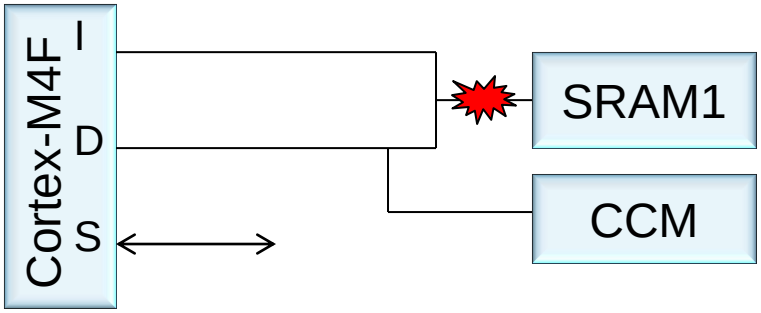
- Config 2



- Access are penalized by:
  - Bus Matrix arbitration when switching between CCM and Flash for data accesses

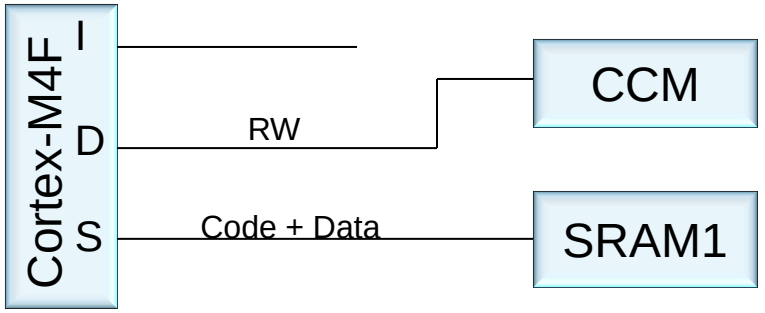
Performance test configuration (2/3)

- Config 3



- Access are penalized by :
  - Convergence of the 2 buses (I-&D- bus) on the same memory,

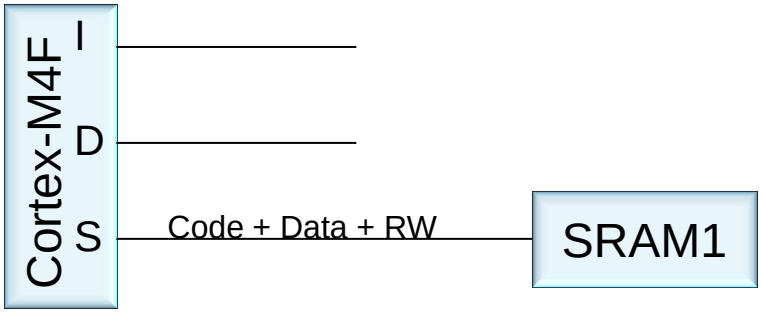
- Config 4



- No wait states inserted as bus are dedicated (no arbitration)

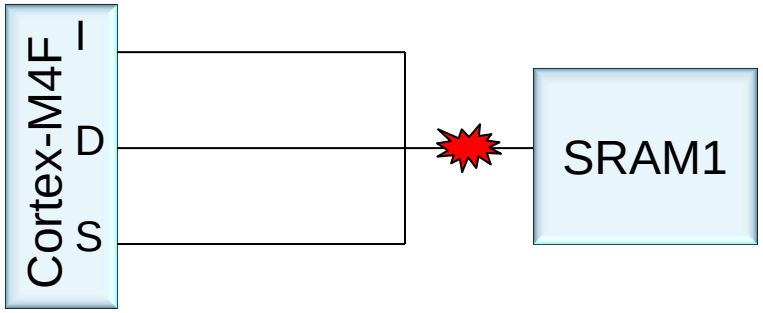
Performance test configuration (3/3)

- Config 5



- No wait states inserted, full SRAM bandwidth is dedicated to program execution
- Access is penalized if :
  - CPU is managing peripherals,
  - DMA transfers to SRAM.

- Config 6



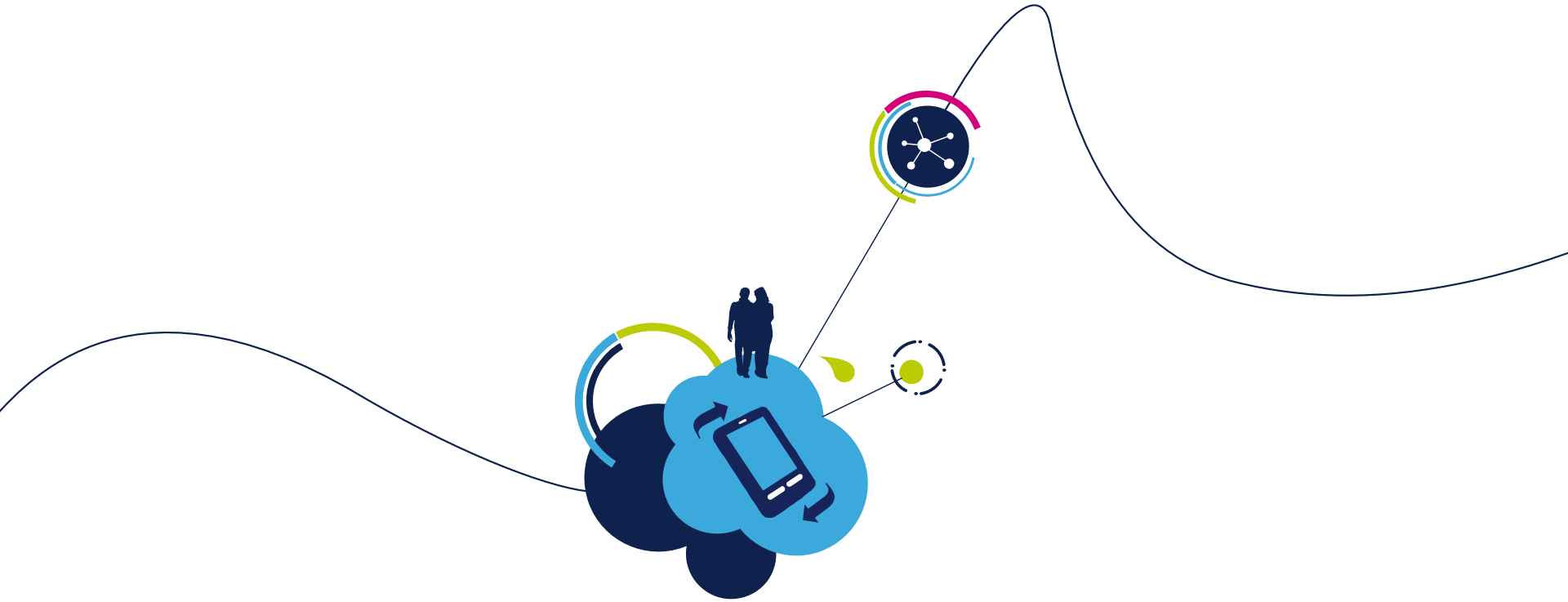
- Access are penalized by :
  - Convergence of the 3 buses on the same memory,
  - Bus Matrix Arbitration

Example execution results

- The best performance are achieved when :
  - No arbitration is inserted,
  - One memory dedicated for each bus.

Configuration	Description	Iterations
Config 1	Code : Flash RAM: SRAM1	106251
Config 2	Code : Flash RAM: CCM	89969
Config 3	Code : SRAM1 (remapped) RAM: CCM	83624
Config 4	Code: SRAM1 (no remap) RAM: CCM	83531
Config 5	Code: SRAM1 (no remap) RAM: SRAM1	83531
Config 6	Code: SRAM1 (remapped) RAM: SRAM1 (on S-Bus)	68890

Contents



AMR
(Absolute Maximum Ratings)

STM32 Datasheets Major update
AMR “Absolute Maximum Rating”

- Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device.

  This is a stress rating only and **functional operation of the device under these conditions is not implied**. Exposure to maximum rating conditions for extended periods may affect **device reliability**.

- AMR section updated to clearly separate voltage and current maximum ratings

STM32 Datasheets Major update
AMR “Absolute Maximum Rating”

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN} (2)	Input voltage on five volt tolerant pin	V_{SS} – 0.3	V_{DD} + 4.0	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. VIN maximum must always be respected. Refer to *Table 8.* for maximum allowed injected current values.

Only Max Must be always respected NOT Minimum

That means we can have “Vin” lower than VSS-0.3Volts while not exceeding -5mA. !

This feature is interesting for mains powered applications to detect Zero Crossing

STM32 Datasheets Major update
AMR “Absolute Maximum Rating” - Voltage

- The true voltage AMR is now given in the AMR voltage characteristics table. This voltage is the **Absolute Voltage.** However, user must also care about current injection and to refer to Current Injection Table.

STM32 Datasheets Major update
AMR “Absolute Maximum Rating” - Current

- The injection information is no table.
- The injection AND the maximu
- When possible, positive injecti

Note 3, 4 and 5 were updated.

Table 8. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	– 25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.19: 12-bit ADC characteristics*.
3. **Positive injection is not possible on these I/Os. A negative injection is induced by VIN<VSS. IINJ(PIN) must never be exceeded. Refer to *Table 7.* for maximum allowed input voltage values.**
4. A positive injection is induced by VIN>VDD while a negative injection is induced by VIN<VSS. IINJ(PIN) must never be exceeded. Refer to *Table 7.* for maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum ΣIINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).

STM32 Datasheets Major update
AMR “Absolute Maximum Rating” - IOs

- The AMR Vin must not be unders
- The allowed Vin operating condit **characteristics** table, with VIH p

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage		–0.3		0.28*(V_{DD}-2 V)+0.8 V	V
	IO FT(1) input low level voltage		–0.3		0.32*(V_{DD}-2 V)+0.75 V	V
V_{IH}	Standard IO input high level voltage		0.41*(V_{DD}-2 V)+1.3 V		V_{DD}+0.3	V
	IO FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V		5.5	V
		V_{DD} ≤ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)		200			mV
	IO FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)			mV
I_{lkg}	Input leakage current (4)	V_{SS} ≤ V_{IN} ≤ V_{DD} Standard I/Os			±1	µA
		V_{IN}= 5 V, I/O FT			3	
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. FT = Five-volt tolerant. In order to sustain a voltage higher than VDD+0.3 the internal pull-up/pull-down resistors must be disabled.

STM32 Datasheets Major update
New section added

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 45*

Table 45. I/O current injection susceptibility

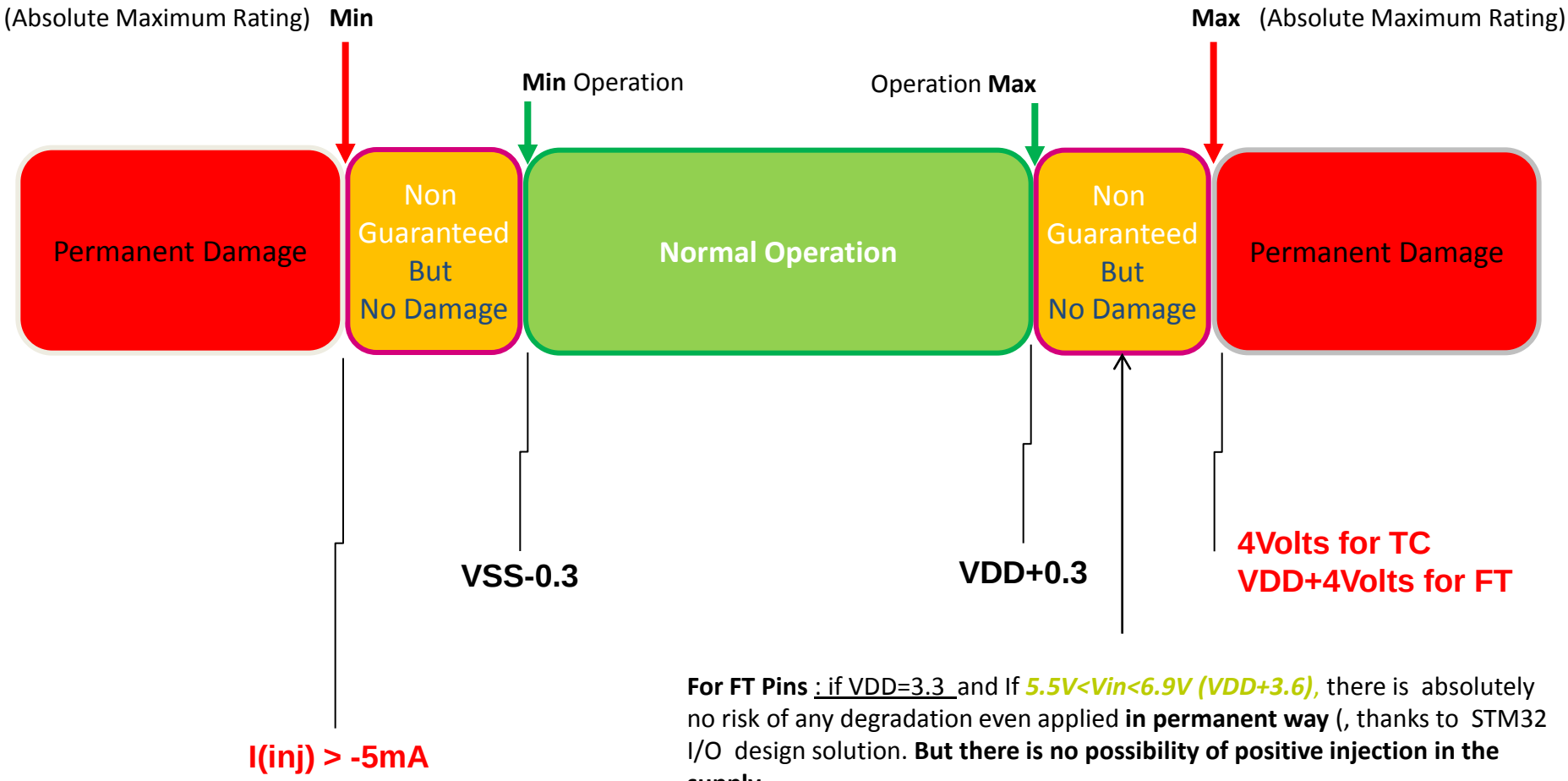
Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Competition positioning
AMR “Absolute Maximum Rating” Voltage

	Item description	Value
STM32	**Input voltage on five volt tolerant pin** **Input voltage on any other pin**	**V_{SS}-0.3 to V_{DD}+4V** **V_{SS}-0.3 to 4V**
CompetR6	Input voltage (except for ports for 5V tolerant) Input voltage (ports for 5V tolerant)	-0.3 to VCC+0.3V -0.3 to 5.8
CompetR2	Input voltage (except for ports for 5V tolerant) Input voltage (ports for 5V tolerant)	-0.3 to VCC+0.3V -0.3 to 6.5V
CompetN18	Input voltage (only valid when the $_{VDD(IO)}$ supply voltage is present) • 5V tolerant I/O pins • ADC/DAC pins and digital I/O pins configured for an analog function • USB pins	 -0.5 to 5.5V TBD to $V_{DDA(3V3)}$ TBD to TBD
CompetA32	Voltage on Input Pin with respect to Ground except … with respect to Ground for …	 -0.3 to 5.5V -0.3 to 3.6V
CompetF56	Digital input voltage Analog input voltage (XTAL) Analog input voltage (ANA0-7,VREF)	V_{SSIO}-0.3 to V_{SSIO}+5.5V V_{SSA}-0.3 to V_{DDA}+0.3V V_{SSA_ADC}-0.3 to V_{SS_ADC}+5.5V
CompetFK	Digital input voltage (except RESET, XTAL) Tamper input voltage Analog, RESET, XTAL input voltage	-0.3 to 5.5V -0.3 to V_{BAT}+0.3V -0.3 to V_{DD}+0.3V
CompetM32	Voltage on any pin that is not 5V tolerant with respect to V_{SS} Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD}≥3V Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD}<3V	-0.3 to V_{DD}+0.3V -0.3 to 5.6V -0.3 to 3.6V

Often specific competitor notes makes this positioning better for STM32

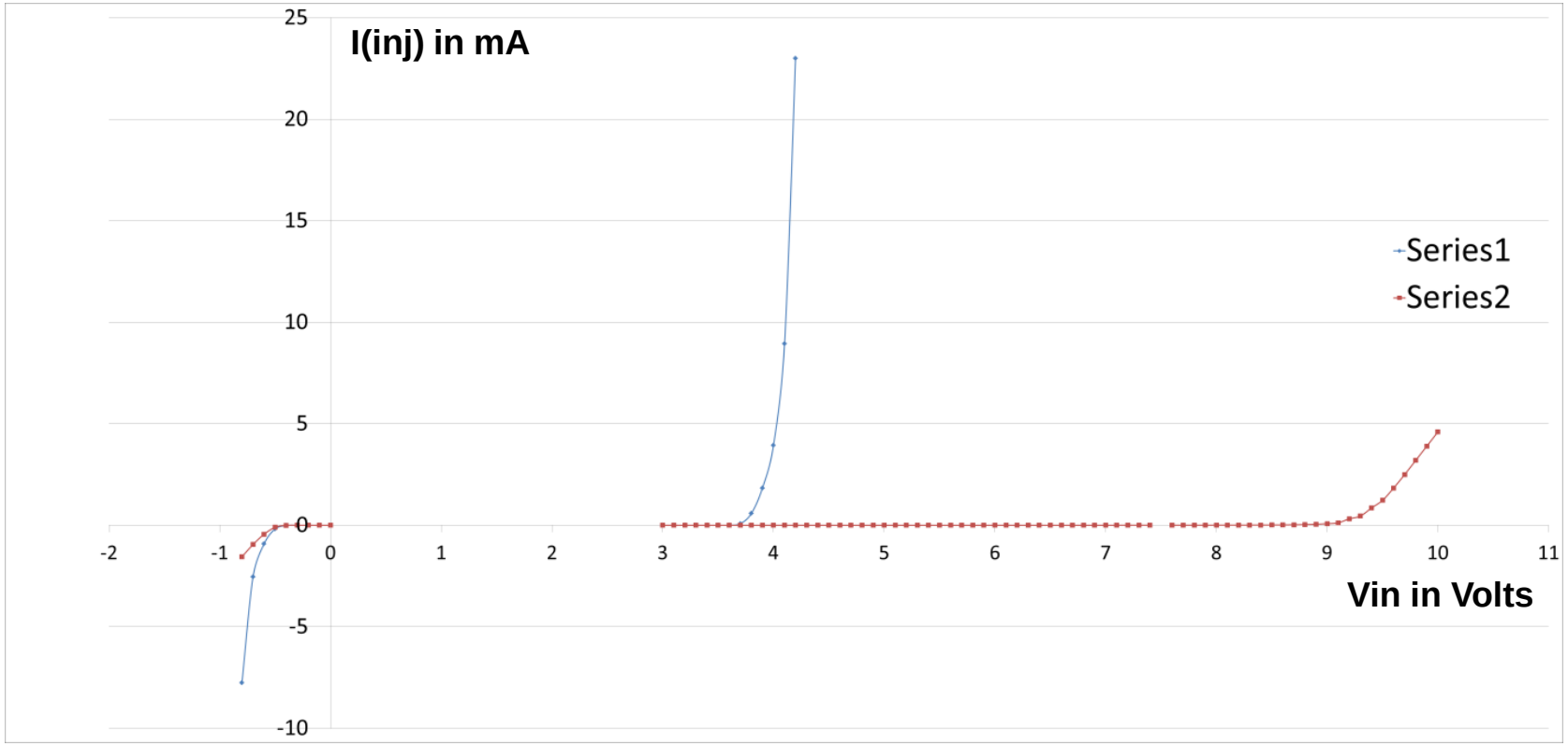
Synthesis



For FT Pins : if VDD=3.3 and If ***5.5V<Vin<6.9V (VDD+3.6)***, there is absolutely no risk of any degradation even applied **in permanent way** (, thanks to STM32 I/O design solution. **But there is no possibility of positive injection in the supply.**

There is only a small consumption observed on the pad signal which has nothing to see with injection. However, between 6.9V<Vin<7.3V, there is no risk if the potential is applied during a short time (AMR Principle)

Typical I/O behavior of two I/Os

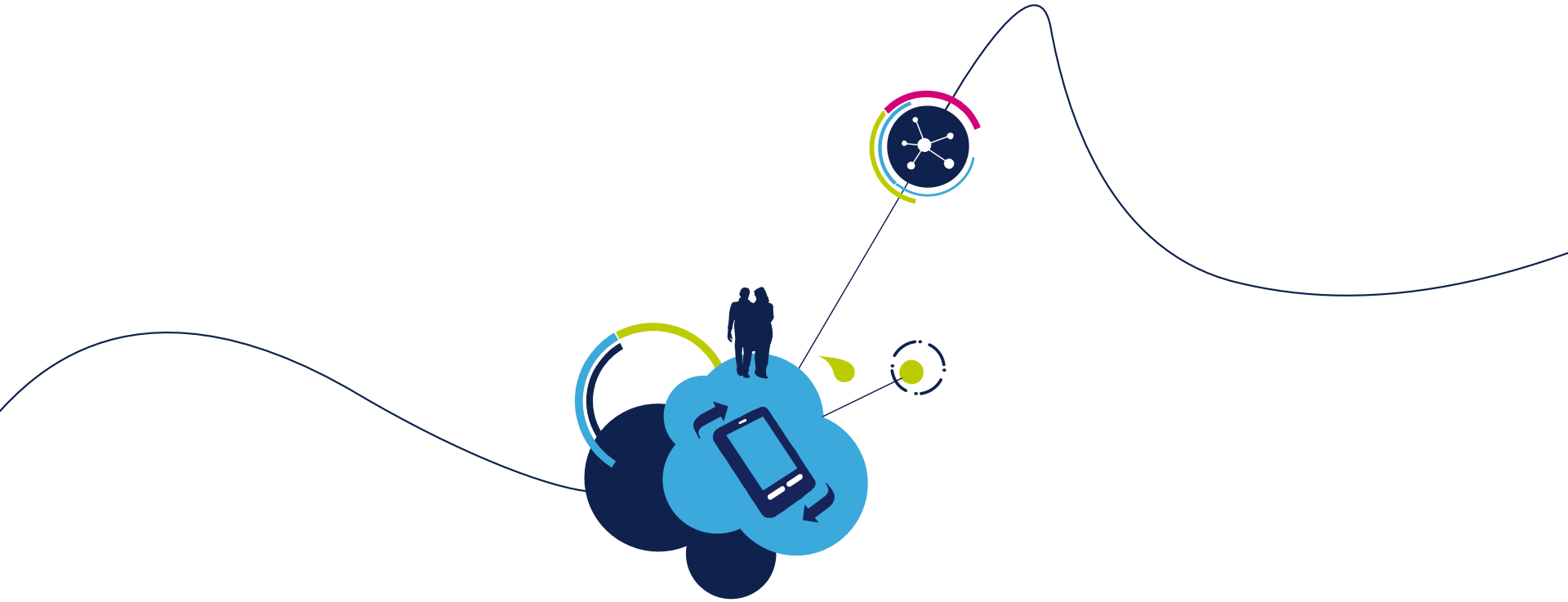


- STM32F1xx device : Vin is applied directly on the pad **without serial limiting resistance**
  - Series1 (blue) = TC I/O
  - Series2 (red) = FT I/O

PA9, PB13 USB V_{BUS} Sensing feature

- **Customer case application:** USB device peripheral application
- **I/O configuration:** V_{BUS} PA9 should be left at default state (floating input), not as alternate function !
- **Observed behavior:** A current of about 200µA is seen on the pad
- **Explanation:**
  - The current observed on V_{BUS} pad is normal and expected with the present design.
  - This is indeed due to the V_{BUS} sensing block where a **current to voltage conversion** is implemented to determine the different sessions.

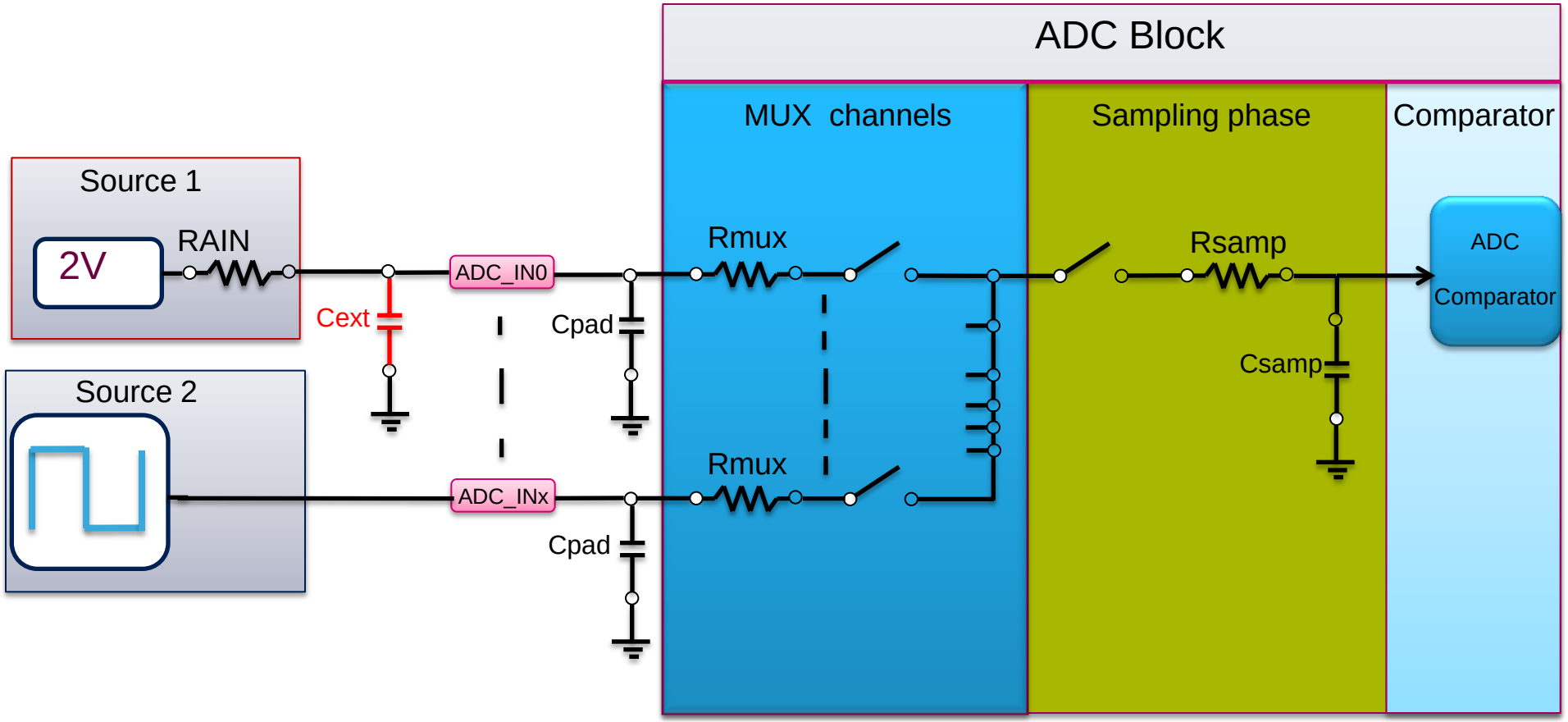
→ This behavior is will be documented in future in our datasheets



ADC

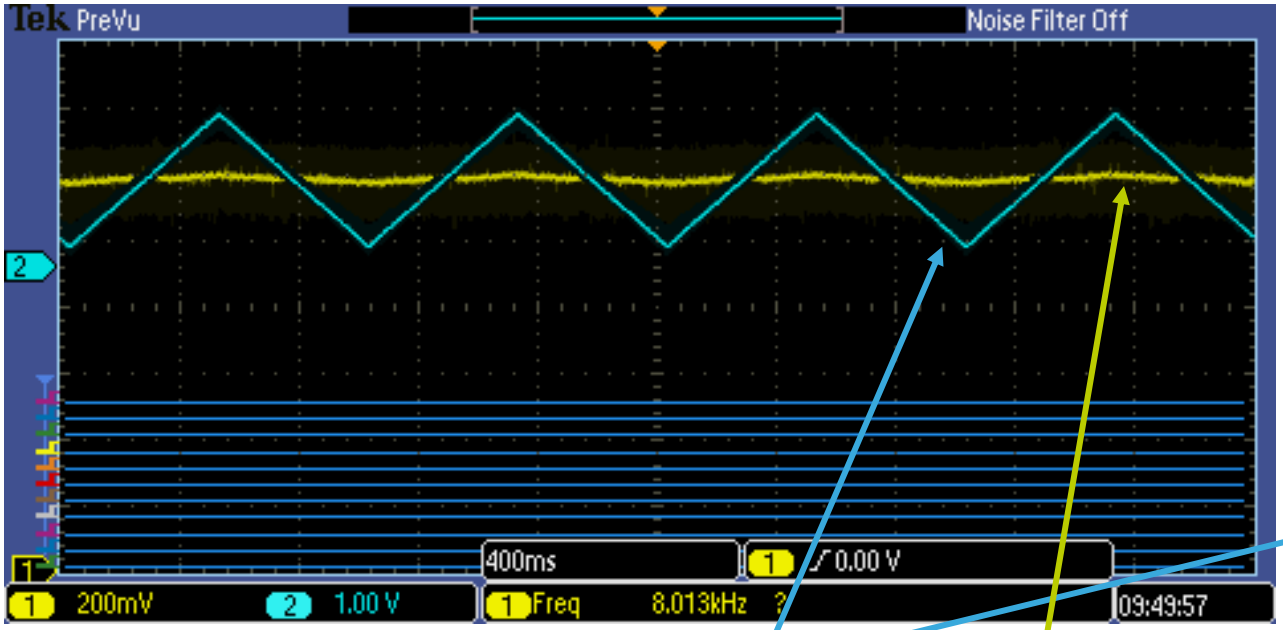
How to choose the right sampling time ?

Typical application case

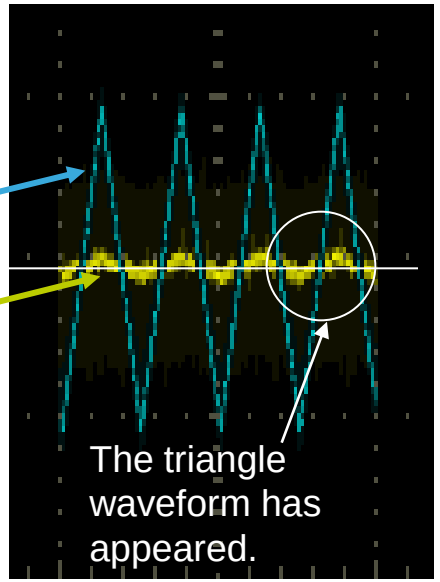


Strange crosstalk behavior

Both ADC_IN0 and ADC_INx are scanned by ADC in continuous mode
R_{AIN} is 33 KOhm .



Zoom



ADC_IN15(PC5) (Y axis)

ADC_IN0(PA0)(Vref)

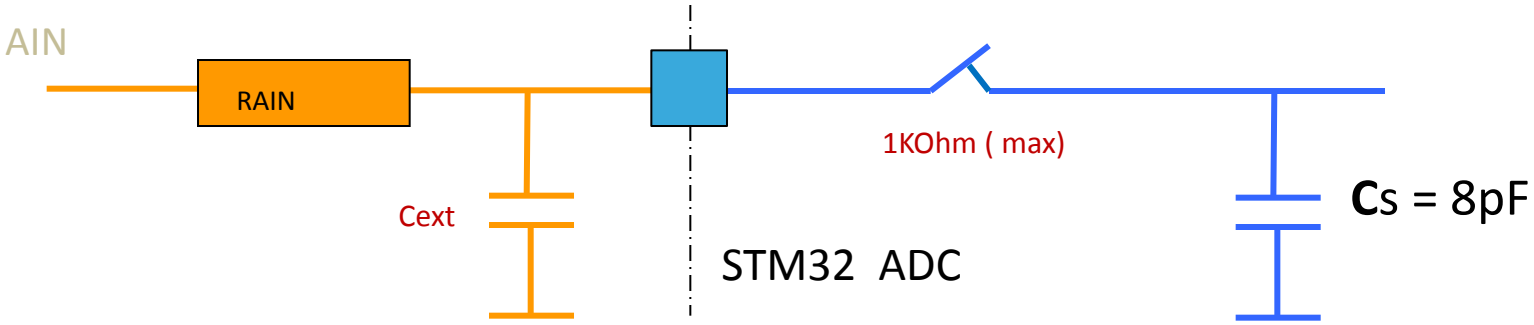
ADC_IN0 must be fixed voltage. But , we observe that it is affected by triangle wave of ADC_INx

Explanation (1/5)

- In STM32F1xx devices, we have a SAR ADC peripheral able to sustain up to 1Msps
- The side effect of any SAR ADC is that the sample capacitor within the ADC **is directly charged by the external signal (*)**, that means if the sample time is insufficient, then the charge left on the sample capacitor by the previous conversion of a channel can affect the accuracy of the channel currently being converted.
- This phenomenon is referred to as channel-to-channel crosstalk and is exactly what has been observed by our experiments.

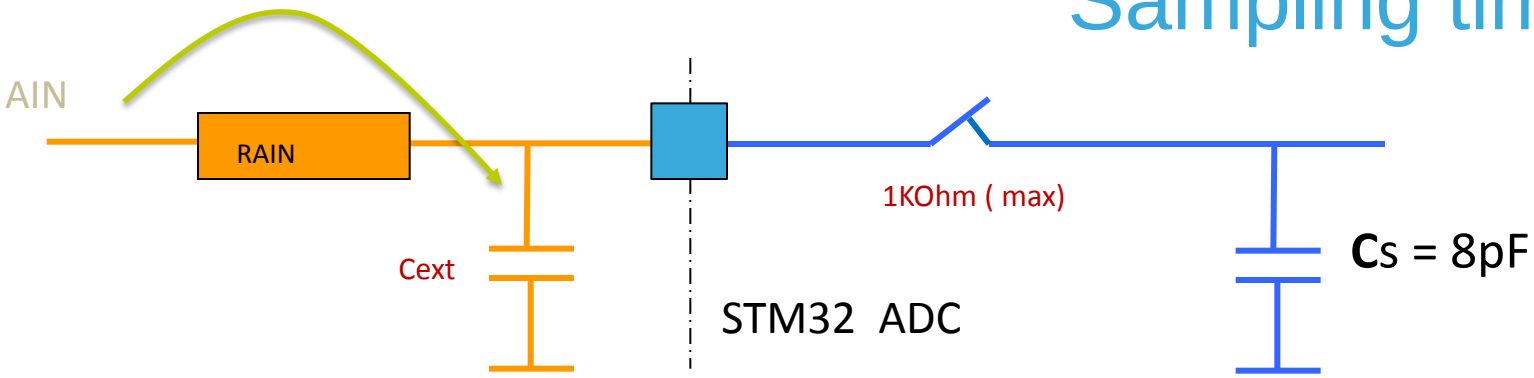
(*) There is not discharge of sample and hold capacitor at the end of the conversion

Explanation (2/5) ADC Input Model



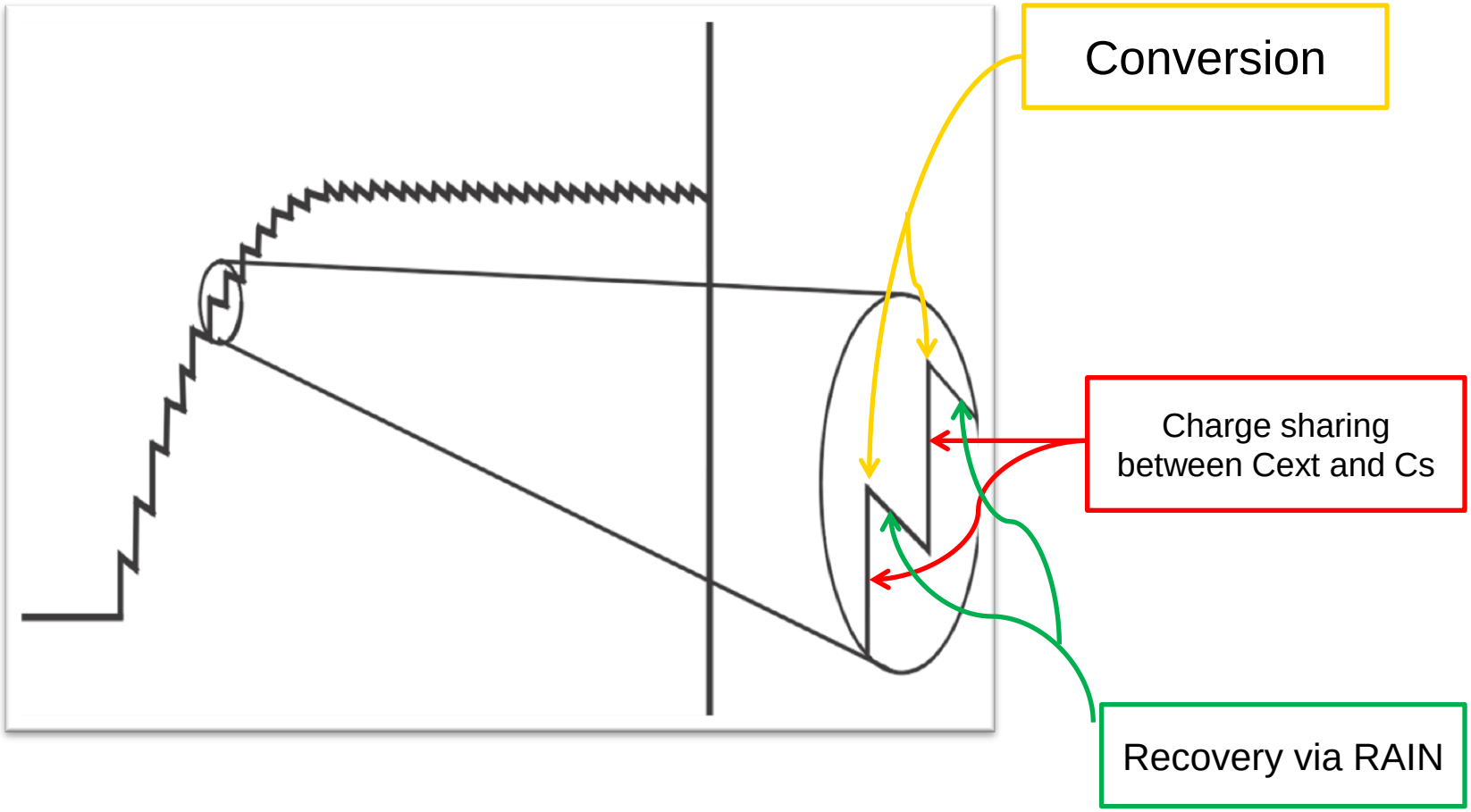
- The Block at right side is the Internal ADC input model and the block at left side is optional and done by the customer/user externally,
- Generally, some users place a large capacitor “Cext” [100nF in this case] from the ADC pin to ground, This capacitor is used to lower the source impedance of the channel as seen by the ADC so that the internal sample capacitor can be charged quickly.
- But this will create a **charge-sharing** process between Cext and Cs, whose RC time constant is primarily determined by the maximum ADC input resistance (1KOhm) and maximum sample capacitance (8pF) of the ADC.
- **As RAIN is increased**, the cutoff frequency created **by RAIN and Cext** will be lowered.

Explanation (3/5) Sampling time

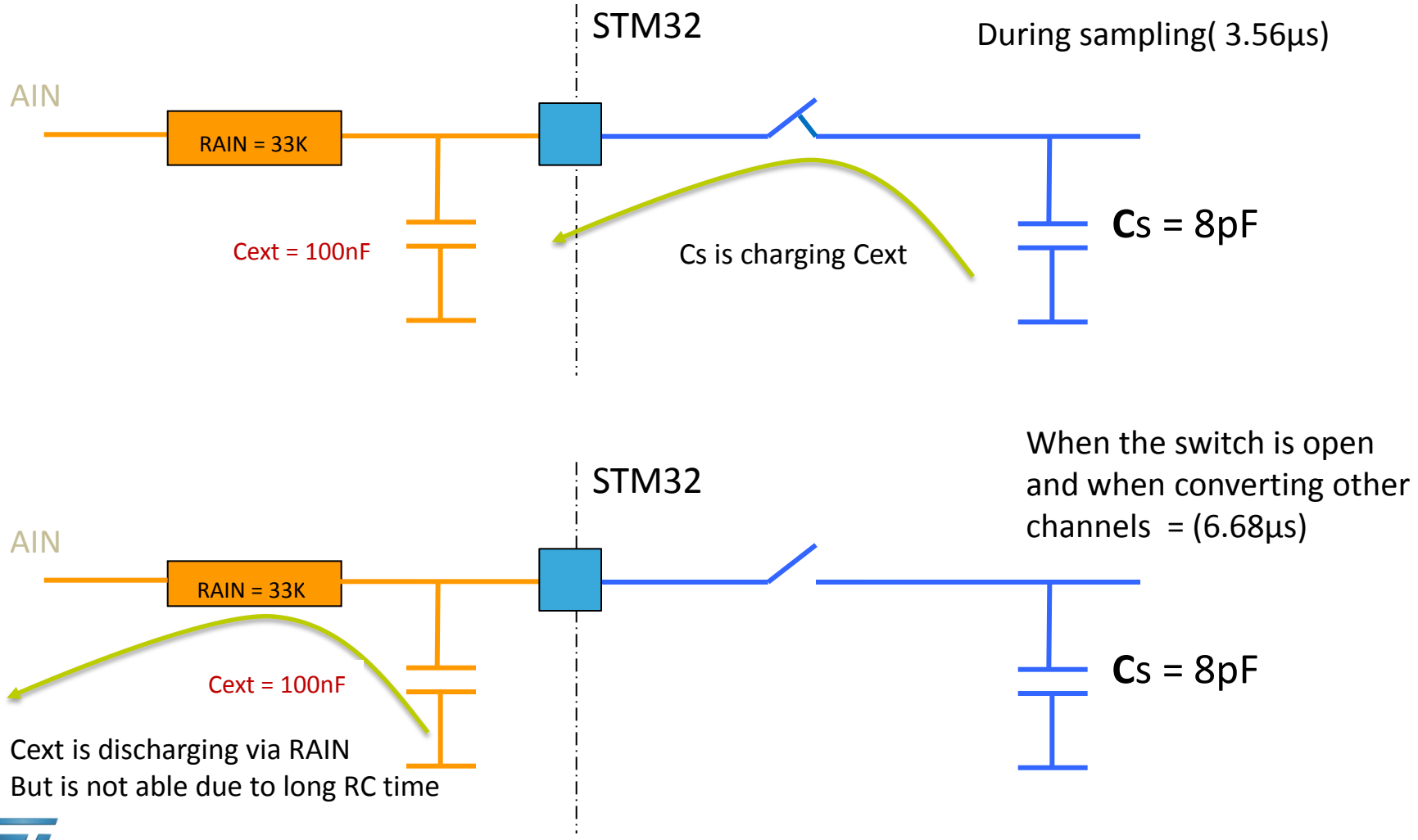


- The Time constant required for an RC circuit to settle to within 1/4 LSB with 12 bits resolution is : ∂ = ln (2 pow (12+2))= 9.7 time constant ~ 10 time constant
- That means in our case, Cext=100nF and RAIN=33KOhm, that channel should sampled/converted not less than each : 10 x 100nF * 33KOhm = **“33ms”**.
- Cext is repeated discharged/charged to Cs via the switch (1KOhm) during sampling time 28.5cycles at 8MHz = 3.56µs without having enough time to be recharged/discharged via RAIN for a whole 33ms.

Explanation (4/5) Charge sharing



Explanation (5/5)
Charge transfer from previous conversion



Sampling time (if C_{ext}=0)

- There is not discharge of sample and hold capacitor at the end of the conversion.
- Sampling is optimized if following rules are achieved.

R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 47* for details			50	kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				8	pF

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 47. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

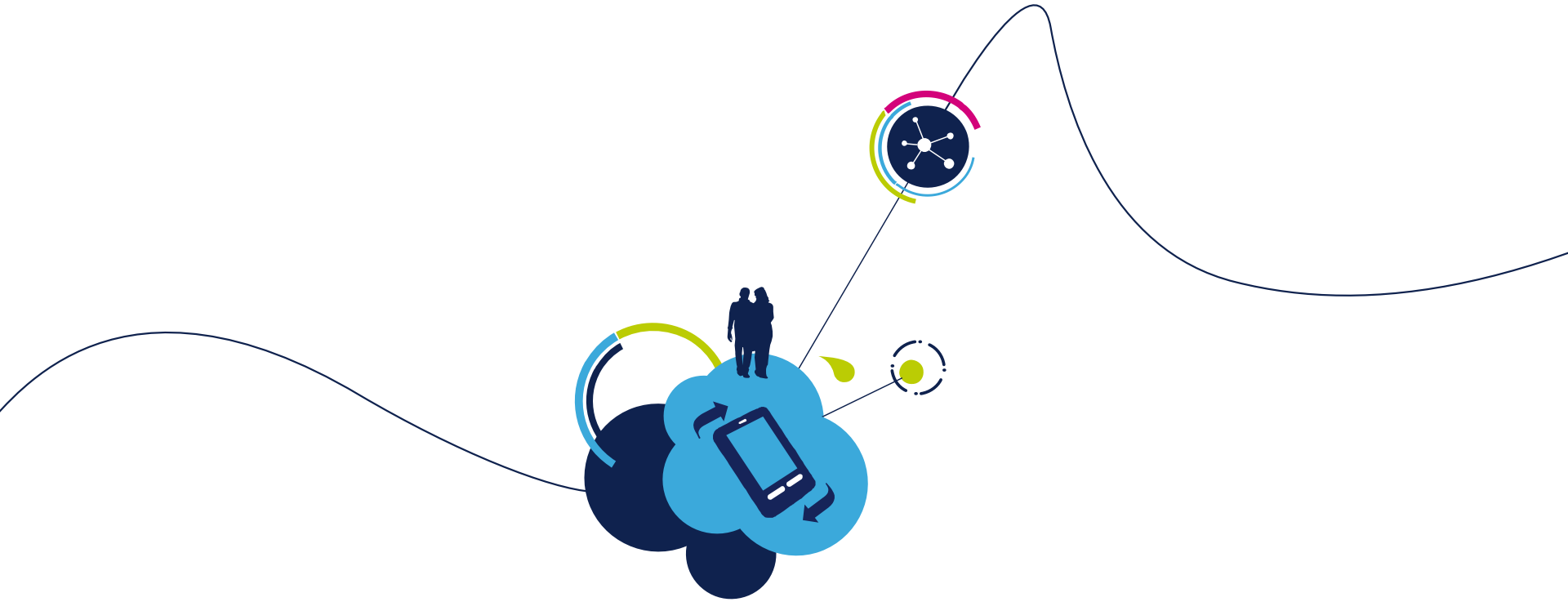
Recommendation & Conclusion

- We can conclude that this issue is coming from inadequate selection of the right sampling time when converting that channel continuously in scan mode and we need to reduce that constant time by different means/methods:

$$T_{Samp} > ln(2^{(12+2)}) * C_{ext} * R_{AIN}$$

$$C_{ext} \geq 2^{(12+2)} * C_S = 16384 * C_S$$

1. Put a very large C_{ext} > 132nF
2. Reducing R_{AIN} to match the selected timing of conversion
3. Removing C_{ext} (100nF) capacitor, so the new constant time will be only [(R_{AIN} +1KOhm) * C_S] * 10
4. Increasing the sampling/conversion period of the channel in the total scan more (this may be not acceptable in the application)
5. Add in the scan sequence as sampling of a channel connected to VSSA/VREF- so the C_S will be discharged quickly after each conversion (this may be not acceptable for in some applications)

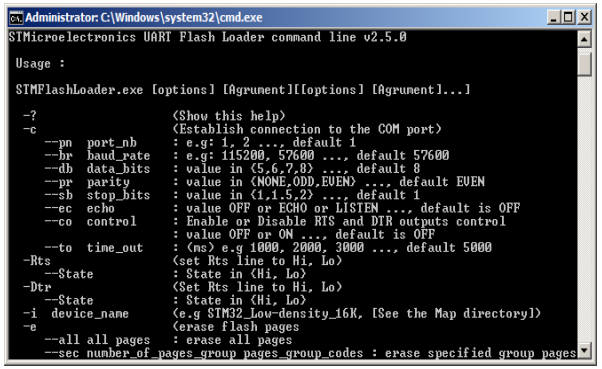


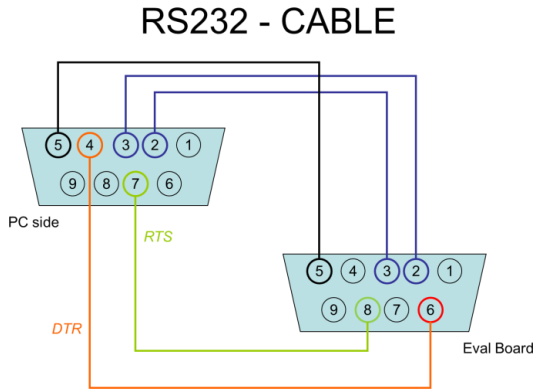
PC Software update (Flash Loader & DFuSe)

life.augmented

PC Software Misc updates

- **Flash Loader demonstrator** v2.5.0 **(On Web)**
  - Support of new devices
  - Command line version manage automatic entry in System-Memory mode from PC & **all sources files are provided now including DLLs.**





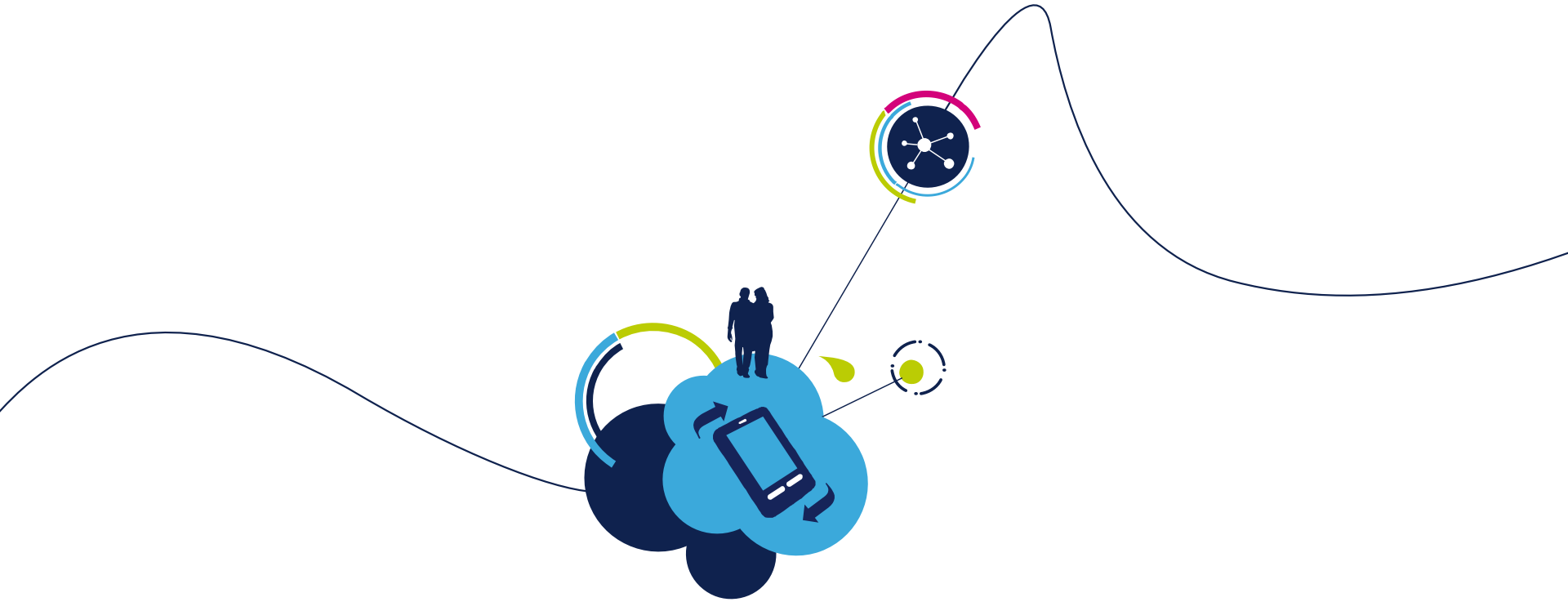
  - RTS and DTR signals should **control Boot0 and Reset pins** on the evaluation board (see STM32F2/4 Evaluation board as reference)

- **DFuSe** v3.0.3 **(On Web in June 2012)**
  - Support of new devices
  - **Add of new Command line version for Automatic update without GUI** !

Contents

Last Period Most interesting issue

- The customer is seeing on his board using STM32F2 series that sometimes a **hard-fault** is triggered and suspected that the Flash or ART has a limitation with a special assembly sequence.
- However on ST Evaluation board, he can not replicate the case.
- Root cause: After long investigations and simulations to reproduce the case , we found that Instead of putting 2.2**µF** caps on V_{CAP} pins, we found **2.2nF** !!



END