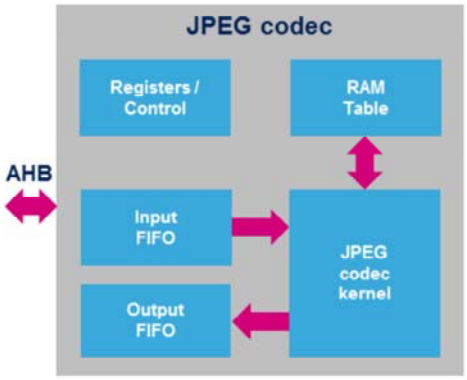
Hello, and welcome to this presentation of the STM32 JPEG codec. I will present the features of this encoder/decoder used for graphics-oriented applications.

Overview



- Provides hardware acceleration for JPEG encoding and decoding
  - Encoding and decoding support
  - Header parsing and generation
  - Fully programmable JPEG tables

Application benefits

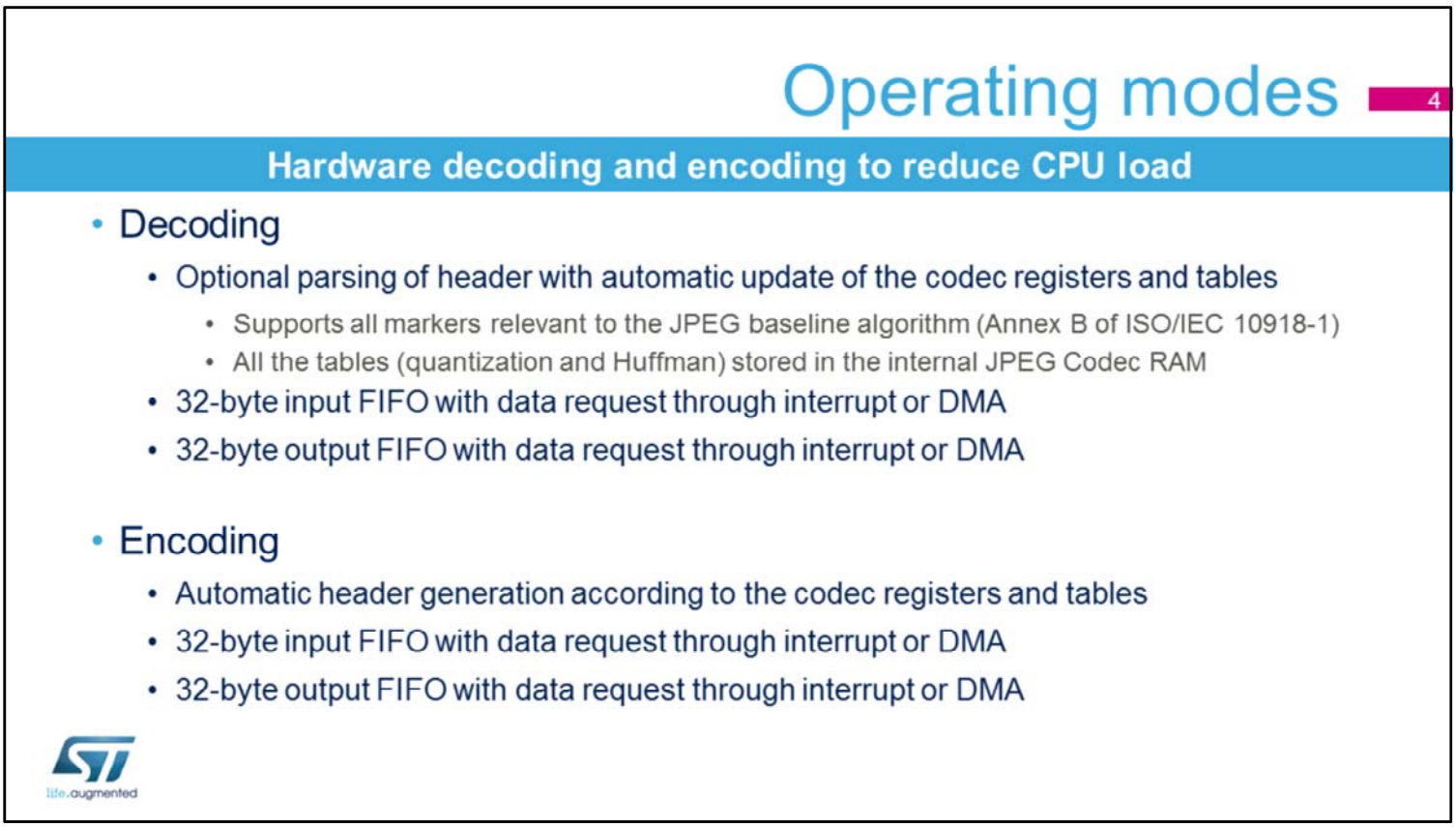
- Fully hardware JPEG codec
- Fast encoding/decoding (one data pixel per cycle)
- Simple integration without CPU load
- Can be used for M-JPEG video playback

The JPEG codec integrated inside STM32 products is an hardware accelerator for JPEG image encoding and decoding. It includes a hardware JPEG header generator and parser for automatic JPEG file handling. All the JPEG tables needed for both encoding and decoding are fully programmable.
As the JPEG codec is fully implemented in hardware, it delivers one data pixel per cycle without any CPU load. Thanks to this flexible feature and its high level of performances, the JPEG codec can be used for M-JPEG video playback.

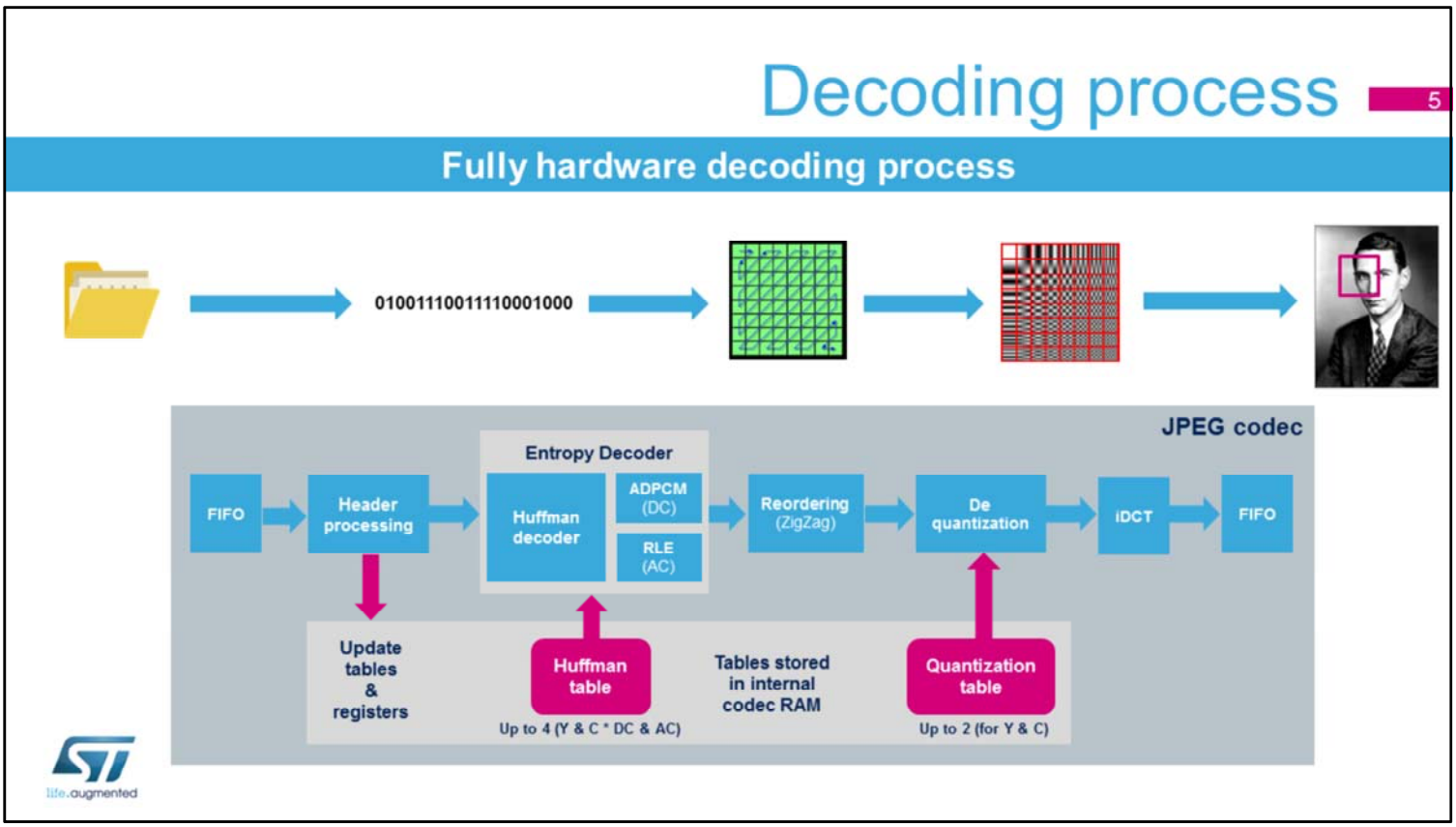
Key features

- Main functions
  - 8 bits per channel for pixel depth
  - Encode/decode support (not simultaneous)
  - Single clock per pixel data encoding and decoding
  - Support for JPEG header generation and parsing
- Flexible IP
  - Up to four programmable quantization tables
  - Fully programmable Huffman tables (two AC and two DC)
  - Fully programmable minimum coded unit (MCU)

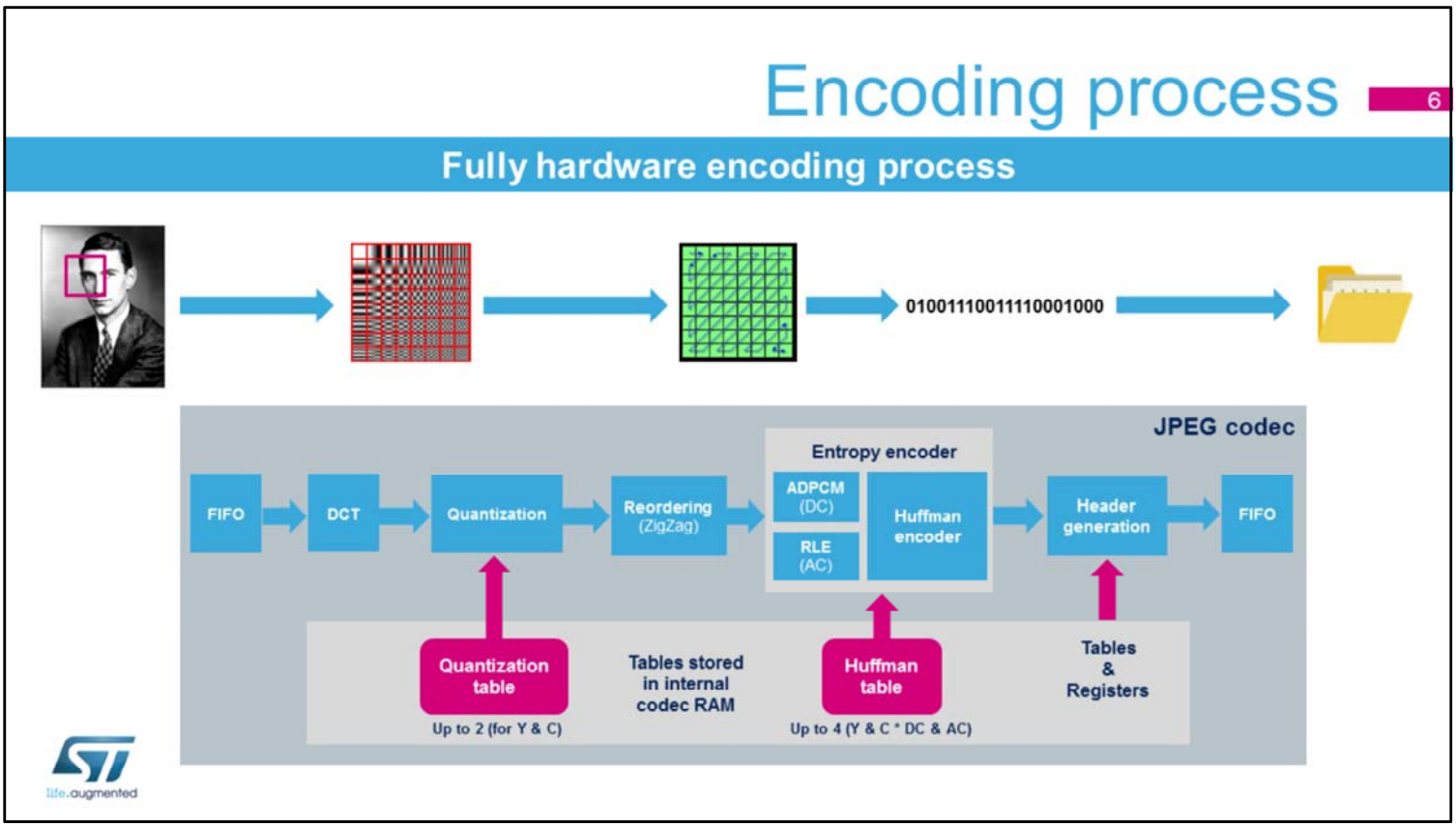
The JPEG codec works with a standard pixel depth of 8 bits per channel for pixel depth. Encode and decode processes are fully implemented in hardware but cannot operate simultaneously. Encoding and decoding processes are very efficient allowing a throughput of 1 pixel data per clock cycle. JPEG headers can be handled automatically without any CPU load thanks to the embedded header parser and generator.
The JPEG tables needed by the codec are fully programmable. The codec supports up to four quantization tables and four Huffman tables.



The JPEG codec has two operating modes for decoding and encoding.
During decoding operations, the JPEG header can be automatically parsed. The codec supports all the makers relevant to the JPEG baseline algorithm. All the tables stored in the header are automatically copied into the local codec RAM. The data file is sent to the codec through a 32-byte input FIFO, and the decoded data are available through a 32-byte output FIFO.
While encoding, the JPEG codec can automatically generate the JPEG header copying its internal RAM content into the JPEG header. The output data file is sent through the 32-byte output FIFO while the picture data are fed into the 32-byte input FIFO.



The decoding process follows the JPEG baseline algorithm: The file data are sent to the input FIFO. The file header is parsed and the corresponding internal RAM tables are updated. Once the header has been parsed, an interrupt can be raised. The compressed data are sent through the entropy decoder to generate the 8 by 8 Minimum Coded Units (MCUs) using the zigzag ordering. The resulting 8x8 tables are de-quantified and transformed through an inverse DCT (iDCT) into the original picture data.



The encoding process works in a similar way:
If the header needs to be generated, the internal tables are copied into the output FIFO with the relevant JPEG markers.
Once generated, the picture data to be compressed are sent through the input FIFO by 8x8 pixel blocks. The original data are transformed through a DCT and the resulting matrix is quantified thanks to the user-programmed quantification table.
The 8x8 transformed table is send as a bit stream using the zigzag algorithm. The data are then processed by the entropy encoder and the compressed stream is sent through the output FIFO.

Interrupts and DMA

Interrupt event	Description
Input FIFO threshold	Input FIFO threshold reached
Input FIFO not full	Input FIFO not full, at least a 32-bit value can be written
Output FIFO threshold	Output FIFO threshold reached
Output FIFO not empty	Output FIFO not empty, at least a 32-bit value can be read out
End of conversion	JPEG processing finished
Header parsing done	End of the header parsing

DMA requests can be generated on FIFO threshold events

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The JPEG codec has 6 interrupt sources:
Input FIFO Threshold and input FIFO Not Full flags are used to manage the input FIFO either by the CPU or DMA.
Output FIFO Threshold and output FIFO Not Empty flags are used to manage the output FIFO either by the CPU or DMA.
End of Conversion flag indicates the end of the JPEG process.
Header Parsing Done flag indicates the end of the header parsing operation.

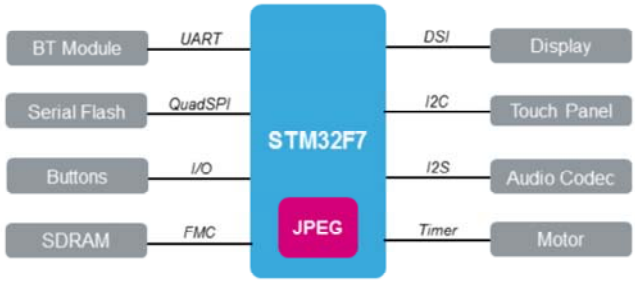
Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Stop	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

The JPEG codec is active in Run and Sleep modes. A JPEG Codec interrupt can cause the device to exit Sleep mode . In Stop mode, the JPEG codec is frozen and its registers content is kept. In Standby mode, the JPEG codec is powered-down and it must be reinitialized afterwards.

Application examples

- Home appliance including connectivity and HMI:



- JPEG codec can decompress
  - JPEG images for HMI
  - M-JPEG video for tutorial playback

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Wearable applications require low-power management functions together with a high-quality user interface. In this scope, the JPEG codec can be used to decode compressed background images, or user pictures, or even to playback certain videos for tutorials.

Related peripherals

- Refer to these trainings linked to this peripheral:
  - RCC (JPEG clock control, JPEG enable/reset)
  - Interrupts (JPEG interrupt mapping)
  - DMA (JPEG data transfer)

You can refer to the training slides related to RCC, interrupts, DMA and GPIO for additional information.

Comparison across STM32F series

JPEG features	STM32F0	STM32F1	STM32F2	STM32F3	STM32F4	STM32F7
Number of instances	0	0	0	0	0	1
Maximum speed	N/A	N/A	N/A	N/A	N/A	216 MHz

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The JPEG codec is available in the STM32F7 series.

References

- For more details, please refer to:
  - ISO/IEC 10918-1 standard

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For more details, please refer to the ISO/IEC 10918-1 standard.