1. Description

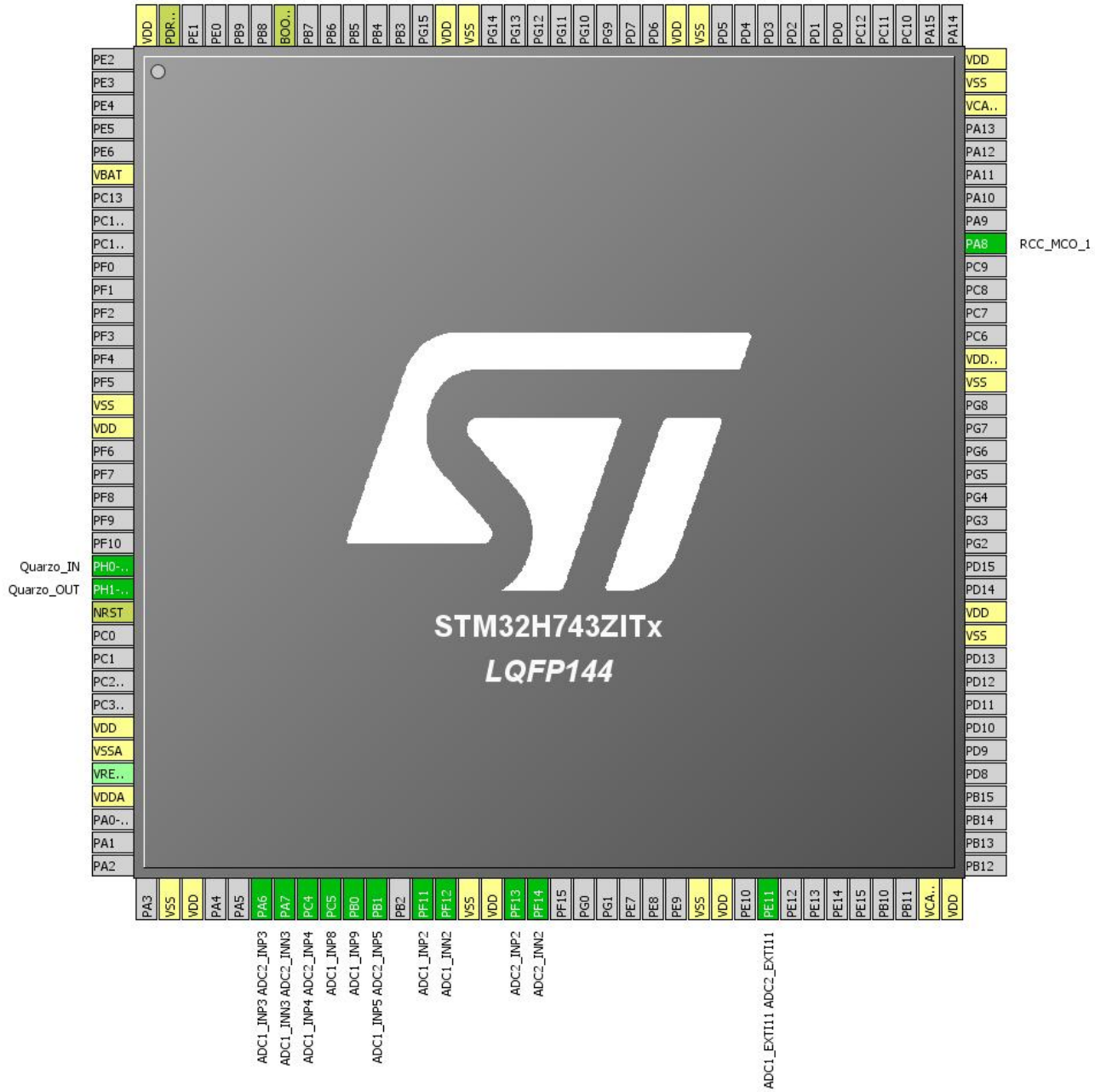
1.1. Project

Project Name	Prova_01
Board Name	Prova_01
Generated with:	STM32CubeMX 4.25.0
Date	05/09/2018

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7x3
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

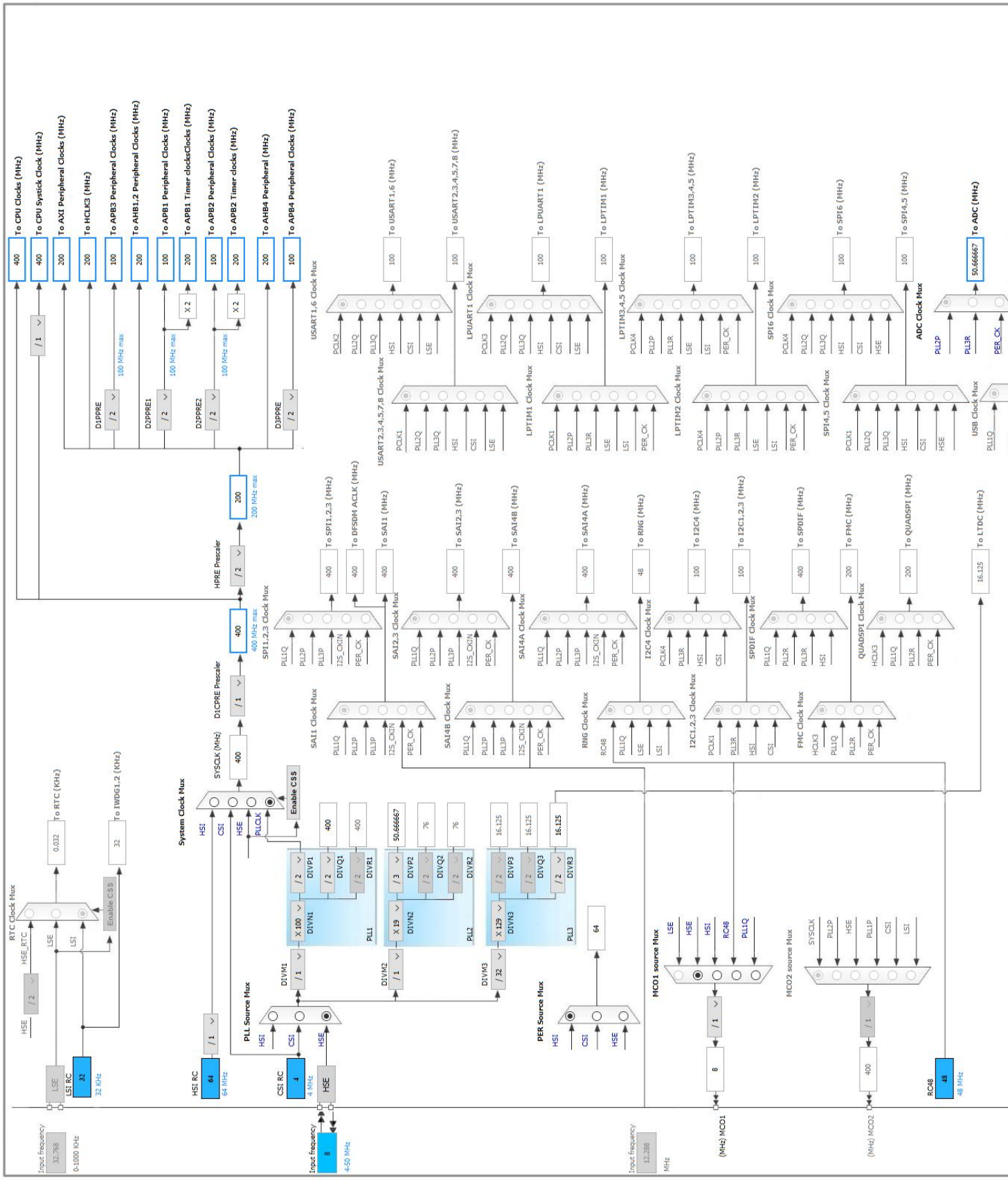


3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN	I/O	RCC_OSC_IN	Quarzo_IN
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	Quarzo_OUT
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
42	PA6	I/O	ADC1_INP3, ADC2_INP3	
43	PA7	I/O	ADC1_INN3, ADC2_INN3	
44	PC4	I/O	ADC1_INP4, ADC2_INP4	
45	PC5	I/O	ADC1_INP8	
46	PB0	I/O	ADC1_INP9	
47	PB1	I/O	ADC1_INP5, ADC2_INP5	
49	PF11	I/O	ADC1_INP2	
50	PF12	I/O	ADC1_INN2	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	ADC2_INP2	
54	PF14	I/O	ADC2_INN2	
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	ADC1_EXTI11, ADC2_EXTI11	
71	VCAP1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD33_USB	Power		
100	PA8	I/O	RCC_MCO_1	
106	VCAP2	Power		
107	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
108	VDD	Power		
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN2: IN2 Differential
IN3: IN3 Differential
IN4: IN4 Single-ended
IN5: IN5 Single-ended
mode: IN8
mode: IN9
Conversion Trigger: Regular Conversion Trigger

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	DMA access mode disabled
Delay between 2 sampling phases	1,5 Cycle

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Boost Mode	Enabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	EXTI Line11
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 2

Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	**true ***
Watchdog Mode	Single regular channel
Analog WatchDog Channel	Channel 2
High Threshold	0
Low Threshold	0
Interrupt Mode	Disabled

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. ADC2

IN2: IN2 Differential

IN3: IN3 Differential

IN4: IN4 Single-ended

IN5: IN5 Single-ended

Conversion Trigger: Regular Conversion Trigger

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	DMA access mode disabled
Delay between 2 sampling phases	1,5 Cycle

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved

Boost Mode	Enabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
Rank	1
Channel	Channel 2
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator
mode: Master Clock Output 1

5.3.1. Parameter Settings:

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	16

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range
PLL Fractional Part	0
PLL2 Fractional Part	0

5.4. SYS

Timebase Source: SysTick

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_INN3	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_INP8	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	
	PF11	ADC1_INP2	Analog mode	No pull-up and no pull-down	n/a	
	PF12	ADC1_INN2	Analog mode	No pull-up and no pull-down	n/a	
	PE11	ADC1_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
ADC2	PA6	ADC2_INP3	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC2_INN3	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC2_INP4	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC2_INP5	Analog mode	No pull-up and no pull-down	n/a	
	PF13	ADC2_INP2	Analog mode	No pull-up and no pull-down	n/a	
	PF14	ADC2_INN2	Analog mode	No pull-up and no pull-down	n/a	
	PE11	ADC2_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	Quarzo_IN
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	Quarzo_OUT
	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

nothing configured in DMA service

6.3. BDMA configuration

nothing configured in DMA service

6.4. MDMA configuration

nothing configured in DMA service

6.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7x3
MCU	STM32H743ZITx
Datasheet	030538_Rev1

7.2. Parameter Selection

Temperature	25
Vdd	3.0

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Prova_01
Project Folder	C:\Users\Andrea\Atollic\TrueSTUDIO\STM32_workspace_9.0\Prova_01
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_H7 V1.2.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report