



1. Description

1.1. Project

Project Name	STCubeGenerated
Board Name	custom
Generated with:	STM32CubeMX 6.0.1
Date	09/16/2020

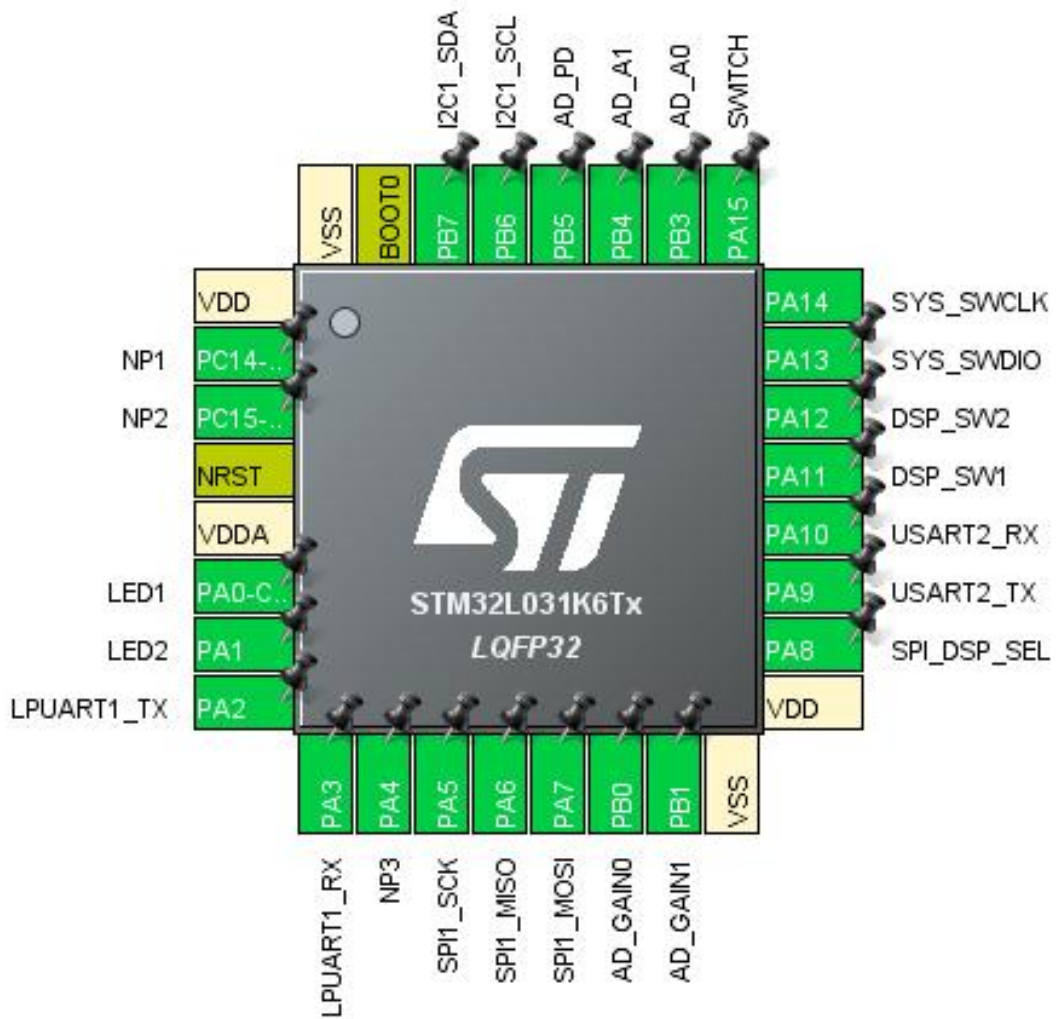
1.2. MCU

MCU Series	STM32L0
MCU Line	STM32L0x1
MCU name	STM32L031K6Tx
MCU Package	LQFP32
MCU Pin number	32

1.3. Core(s) information

Core(s)	Arm Cortex-M0+
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PC14-OSC32_IN *	I/O	GPIO_Input	NP1
3	PC15-OSC32_OUT *	I/O	GPIO_Input	NP2
4	NRST	Reset		
5	VDDA	Power		
6	PA0-CK_IN *	I/O	GPIO_Output	LED1
7	PA1 *	I/O	GPIO_Output	LED2
8	PA2	I/O	LPUART1_TX	
9	PA3	I/O	LPUART1_RX	
10	PA4 *	I/O	GPIO_Input	NP3
11	PA5	I/O	SPI1_SCK	
12	PA6	I/O	SPI1_MISO	
13	PA7	I/O	SPI1_MOSI	
14	PB0 *	I/O	GPIO_Output	AD_GAIN0
15	PB1 *	I/O	GPIO_Output	AD_GAIN1
16	VSS	Power		
17	VDD	Power		
18	PA8 *	I/O	GPIO_Output	SPI_DSP_SEL
19	PA9	I/O	USART2_TX	
20	PA10	I/O	USART2_RX	
21	PA11 *	I/O	GPIO_Input	DSP_SW1
22	PA12 *	I/O	GPIO_Input	DSP_SW2
23	PA13	I/O	SYS_SWDIO	
24	PA14	I/O	SYS_SWCLK	
25	PA15 *	I/O	GPIO_Input	SWITCH
26	PB3 *	I/O	GPIO_Output	AD_A0
27	PB4 *	I/O	GPIO_Output	AD_A1
28	PB5 *	I/O	GPIO_Output	AD_PD
29	PB6	I/O	I2C1_SCL	
30	PB7	I/O	I2C1_SDA	
31	BOOT0	Boot		
32	VSS	Power		

* The pin is affected with an I/O function

5. Software Project

5.1. Project Settings

Name	Value
Project Name	STCubeGenerated
Project Folder	C:\Users\SHudis\Desktop\Projects\LockerScale\Firmware\RTE\Device\STM32L0
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_L0 V1.11.2
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_I2C1_Init	I2C1
5	MX_LPUART1_UART_Init	LPUART1
6	MX_USART2_UART_Init	USART2
7	MX_SPI1_Init	SPI1
8	MX_TIM2_Init	TIM2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L0
Line	STM32L0x1
MCU	STM32L031K6Tx
Datasheet	DS10668_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(AAA700)
Capacity	700.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	10.0 mA
Max Pulse Current	30.0 mA
Cells in series	1
Cells in parallel	1

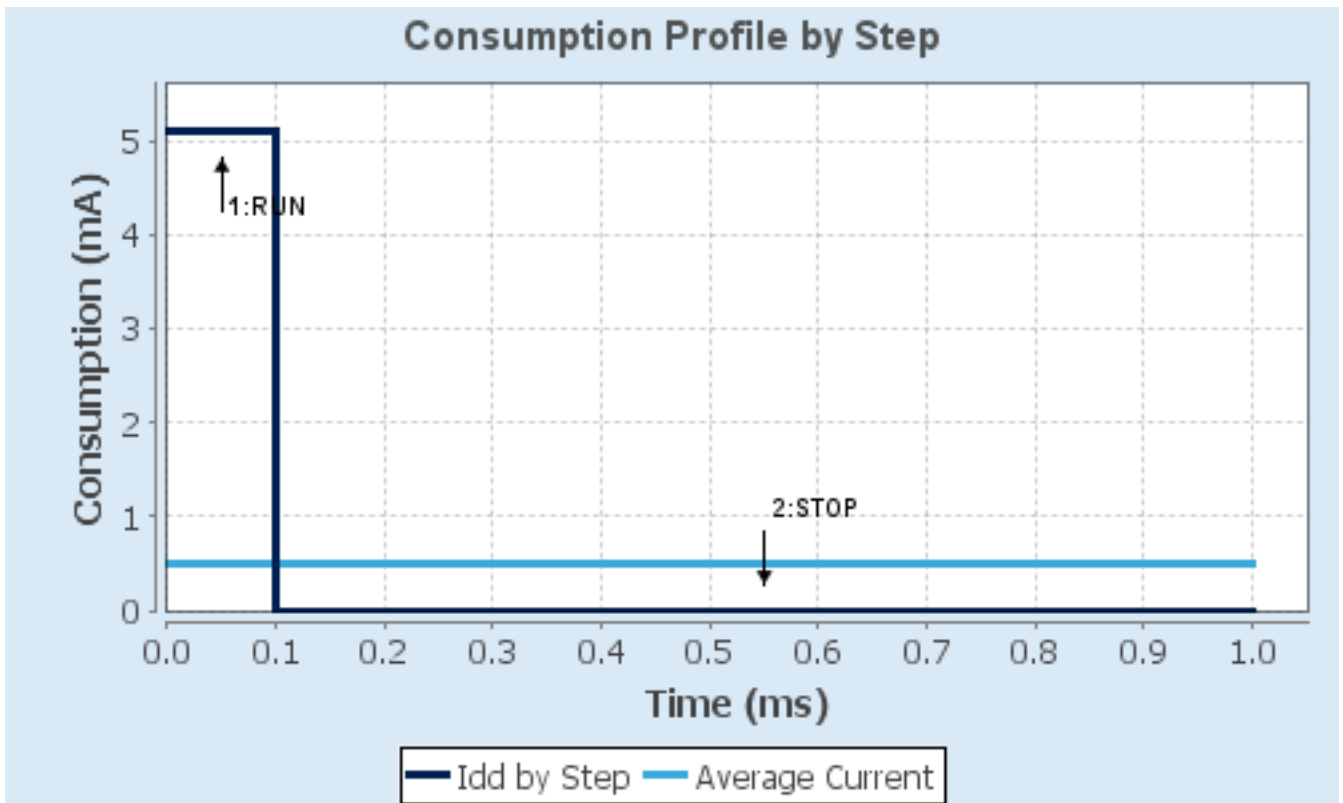
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	n/a
CPU Frequency	32 MHz	0 Hz
Clock Configuration	HSI PLL	ALL CLOCKS OFF
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	5.1 mA	380 nA
Duration	0.1 ms	0.9 ms
DMIPS	30.0	0.0
Ta Max	104.08	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	510.34 μ A
Battery Life	1 month, 26 days, 15 hours	Average DMIPS	30.4 DMIPS

6.6. Chart



7. IPs and Middleware Configuration

7.1. GPIO

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00506682 *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.3. LPUART1

Mode: Asynchronous

7.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200 *
Word Length	8 Bits (including Parity) *
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable

Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Disable *
DMA on RX Error	Disable *
MSB First	Disable

7.4. RCC

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Buffer Cache	Enabled
Prefetch	Disabled
Preread	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.5. SPI1

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	12.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SYS

mode: Debug Serial Wire

Timebase Source: SysTick

7.7. TIM2

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	10800-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	10000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. USART2

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
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TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Disable *
DMA on RX Error	Disable *
MSB First	Disable

* **User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High *	
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
USART2	PA9	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PC14-OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NP1
	PC15-OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NP2
	PA0-CK_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NP3
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD_GAIN0
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD_GAIN1
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI_DSP_SEL
	PA11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DSP_SW1
	PA12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DSP_SW2
	PA15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SWITCH
PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD_A0	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD_A1
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD_PD

8.2. DMA configuration

DMA request	Stream	Direction	Priority
LPUART1_RX	DMA1_Channel3	Peripheral To Memory	High *
LPUART1_TX	DMA1_Channel2	Memory To Peripheral	High *
USART2_RX	DMA1_Channel5	Peripheral To Memory	High *
USART2_TX	DMA1_Channel4	Memory To Peripheral	High *

LPUART1_RX: DMA1_Channel3 DMA request Settings:

Mode: **Circular ***
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

LPUART1_TX: DMA1_Channel2 DMA request Settings:

Mode: Normal
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART2_RX: DMA1_Channel5 DMA request Settings:

Mode: **Circular ***
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART2_TX: DMA1_Channel4 DMA request Settings:

Mode: Normal
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte

Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable Interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel 2 and channel 3 interrupts	true	0	0
DMA1 channel 4, channel 5, channel 6 and channel 7 interrupts	true	0	0
TIM2 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash and EEPROM global interrupt	unused		
RCC global interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
SPI1 global interrupt	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		
LPUART1 global interrupt / LPUART1 wake-up interrupt through EXTI line 28	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable Interrupt	true	true	false
Hard fault interrupt	true	true	false
System service call via SWI instruction	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
DMA1 channel 2 and channel 3 interrupts	true	true	true
DMA1 channel 4, channel 5, channel 6 and channel 7 interrupts	true	true	true
TIM2 global interrupt	true	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware

System Core

Analog

Timers

Connectivity

Computing

DMA ✓

GPIO ✓

IVIC ✓

RCC ✓

SYS ✓

TIM2 ✓

I2C1 ✓

LPUART1 ✓

SPI1 ✓

USART2 ✓

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00140359.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00108282.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00104451.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00182885.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00108286.pdf
Application note	http://www.st.com/resource/en/application_note/DM00112257.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00145318.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00158601.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00150423.pdf

Application note http://www.st.com/resource/en/application_note/DM00209725.pdf
Application note http://www.st.com/resource/en/application_note/DM00209768.pdf
Application note http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note http://www.st.com/resource/en/application_note/DM00206898.pdf
Application note http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note http://www.st.com/resource/en/application_note/DM00226326.pdf
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Application note http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note http://www.st.com/resource/en/application_note/DM00380469.pdf
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Application note http://www.st.com/resource/en/application_note/DM00209772.pdf
Application note http://www.st.com/resource/en/application_note/DM00660597.pdf