



Application Note

AS3993

PLL Loop Filter



Content Guide

1 General Description 3

2 Hardware Description..... 3

3 Board Schematics, Layout and BOM 4

4 Contact Information..... 5

5 Copyrights & Disclaimer..... 6

6 Revision Information 7

1 General Description

AS3993 PLL Loop Filter for fc_{mp} 100 & 125 kHz

2 Hardware Description

Version	fvco	fout	Kvco	fc _{mp}	Nfb	I _{cp}	C1	C2	R2	C3	R3	R. 0x12	fc _{4oln}	fbw _{4oln}	pm _{4oln}	fc _{mp} /fc _{4oln}	ATTEN2F	t _{lock}
	[MHz]	[MHz]	[MHz/V]	[kHz]		[uA]	[pF]	[nF]	[kOhm]	[pF]	[kOhm]	[hex]	[kHz]	[kHz]	[deg]		[dB]	[us]
100k_v1	1765	882.5	36	100	17650	1879	180	3	15	40	70	8E	8.90	15.34	49.9	11.24	33.43	565
125k_v1	1765	882.5	36	125	14120	1561	180	3	15	40	70	8D	9.18	15.91	49.9	13.61	37.99	444
100k_v2	1765	882.5	36	100	17650	1879	150	3.9	15	160	30	36	8.28	14.52	46.3	12.08	37.37	645
125k_v2	1765	882.5	36	125	14120	1561	150	3.9	15	160	30	35	8.53	14.99	46.1	14.65	41.79	516

Notes:

fvco:VCO frequency, $(842.5+922.5)/2=882.5$

Kvco: VCO tuning gain

fc_{mp}: comparison frequency of the PLL

Nfb:division ratio of the feedback divider

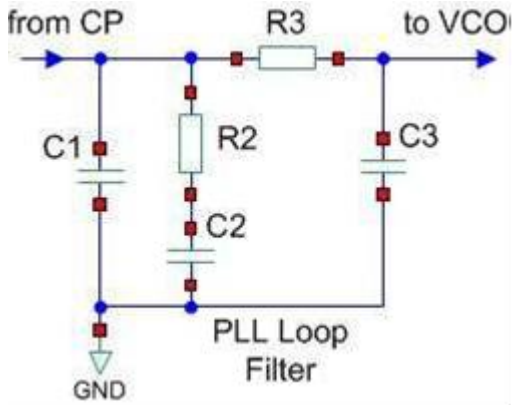
I_{cp}: charge pump current

fc_{4oln}: crossover frequency when the PLL open-loop gain equals to 1

fbw_{4oln}: PLL BW (-3dB)

pm_{4oln}: PLL phase margin

3 Board Schematics, Layout and BOM



4 Contact Information

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6 Revision Information

Changes from 1-00 (2013-Jul-02) to current revision 1-01 (2014-Jul-14)	Page
Update to corporate format	1-5

Note: Page numbers for the previous version may differ from page numbers in the current revision.