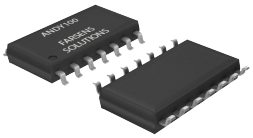
EPC C1G2 COMPLIANT UHF RFID TAG WITH POWER HARVESTING AND SPI COMMUNICATION FOR EXTERNAL LOW POWER SENSORS AND ACTUATORS

Check for samples: ANDY100



FEATURES

- **860MHz-960MHz operation**
- **EPC Class-1 G2 compliant**
- **ISO 18000-6 Type C compliant**
- **96-bit EPC**
- **32-bit TID**
- **Password protected *Kill* command**
- **Password protected *Access* command**
- **Forward link data rates: 26.7kbps to 128 kbps**
- **Return link data rates: 40 to 640 kbps**
- **Return link modulations: FM0 and Miller subcarrier (2, 4, 8)**
- **1.2V, 1.8V and 2.5V regulated outputs**
- **SPI master mode communication for external sensors**
- **Extended temperature range: -30°C to +85°C**

APPLICATIONS

- **Wireless identification**
- **Energy harvesting**
- **Batteryless wireless sensors/actuators**
- **TPMS (Tire Pressure Monitoring Systems)**
- **Cold chain monitoring**
- **Orientation monitoring**
- **Fill level monitoring**
- **Open/close detection**

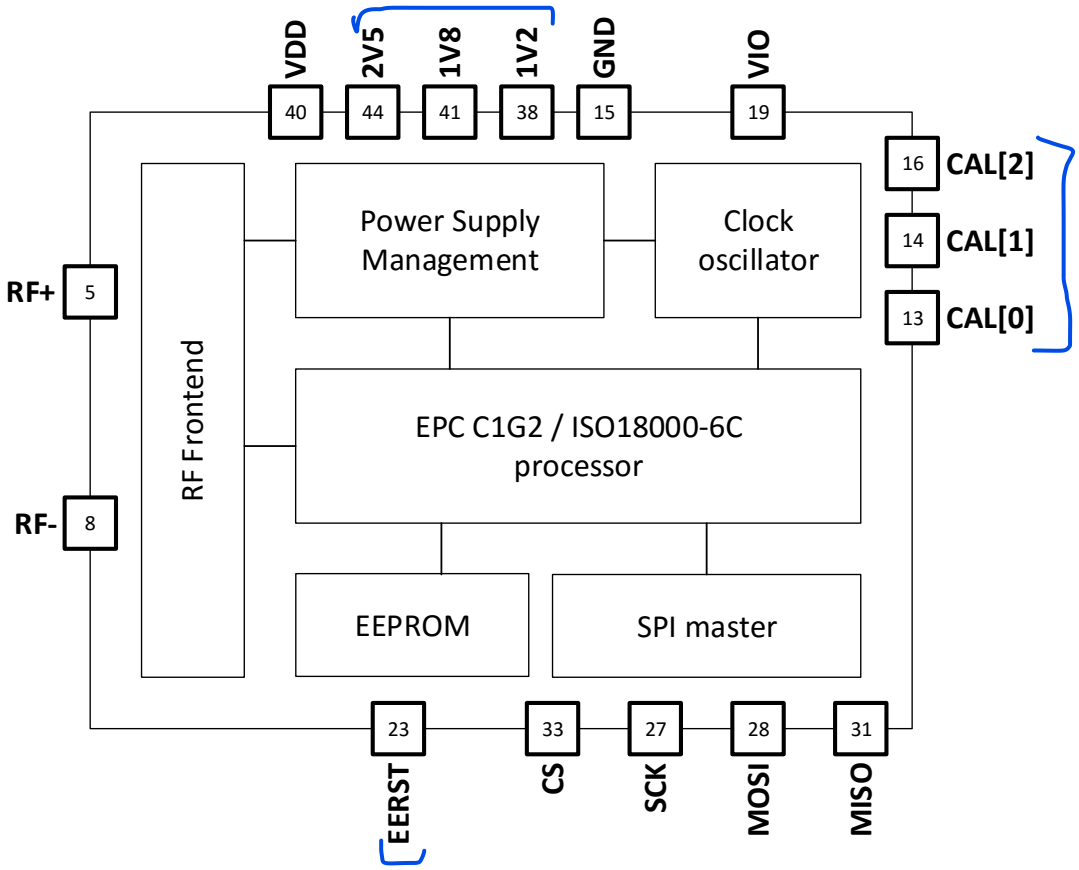
DESCRIPTION

ANDY100 is an EPC Class-1 Generation-2 (C1G2) RFID tag IC which is compliant with ISO/IEC 18000-6 Type C. The chip offers advanced capabilities leading to a performance beyond that of standard RFID tags by including sensor measurements. The IC operates in a fully passive mode harvesting energy from the RF beam emitted by the reader.

ANDY100 includes a non volatile EEPROM to store unique identifiers and passwords for item identification and data protection operations. The memory includes a 96-bit length *Electronic Product Code* (EPC) supporting EPCGlobal Tag Data Standards. The memory also includes a 32-bit length *Tag IDentifier* (TID) supporting ISO/IEC 15963 class-identification. Separate 32-bit length Kill and Access paswords are also included supporting protected kill and data access operations.

Additionally, ANDY100 supports extending the classic functionality of C1G2 tags by attaching an external sensor to the IC. ANDY100 includes the necessary power supply management circuitry to supply external sensors with the energy harvested from the RF field. It also includes a SPI master module to communicate with a sensor, trigger measurements and get the measured data prior to backscattering the obtained value to the reader. All the SPI operations are commanded by the reader using standard memory access commands making the system directly compatible with any standard C1G2 RFID system.

BLOCK DIAGRAM



The functional block diagram of ANDY100 is shown in figure . The RF frontend provides the core RFID functionality, including energy harvesting from the RF field, demodulation of *Amplitude Shift Keying* (ASK) symbols in the forward link and modulation of the impedance of the IC for backscattering data through the reverse link.

The harvested energy is managed by a power supply management unit. This unit includes several low dropout regulators to provide stable supply voltages for internal circuitry and external devices. Regulated voltages of 1.2V, 1.8V and 2.5V are available. The VIO pin sets the reference level for digital input/output signals. It can be connected to any of the regulated voltage outputs or to an external power source.

An application specific digital processor handles the ISO/IEC 18000-6 Type C air protocol managing the non volatile EEPROM according to the standard. The system clock for the digital processor is generated in the integrated clock oscillator.

The clock oscillator requires trimming in order to achieve the precission required by the system. There are three trimming pins for that purpose: CAL[2:0]. In order to facilitate the integration of the IC in the system, two versions of the ANDY100 IC are distinguished: ANDY100U and ANDY100D. For proper operation, all the calibration pins have to be connected either to VIO (ANDY100U) or to GND (ANDY100D).

The digital processor also controls a SPI master module. The SPI master module is used to control and retrieve data from external digital sensors. The operations of the SPI is commanded through standard memory access commands included in the ISO/IEC 18000-6 Type C standard.

The EERST pin can be used to erase all the content of the EEPROM. However, this operation is only recommended for advanced users. Once the EEPROM has been erased, the EPC length defined in the PC bits and the actual length of the EPC will not match. Most readers will not recognize the tag until the correct PC word is programmed again. For this purpose proprietary tools have to be used. For normal operation, it is recommended to connect EERST to GND, so that the EEPROM will operate according to the ISO/IEC 18000-6 Type C standard.

PIN DESCRIPTION

Figures 1 and 2 show the pin diagram of ANDY100 for the available packages. Note that there are several pins that are internally not connected to anything. These pins are noted as nc. Moreover, there are also several reserved inputs and outputs that should be left floating or connected to ground. These pins are noted as float and gnd respectively.

QFN48

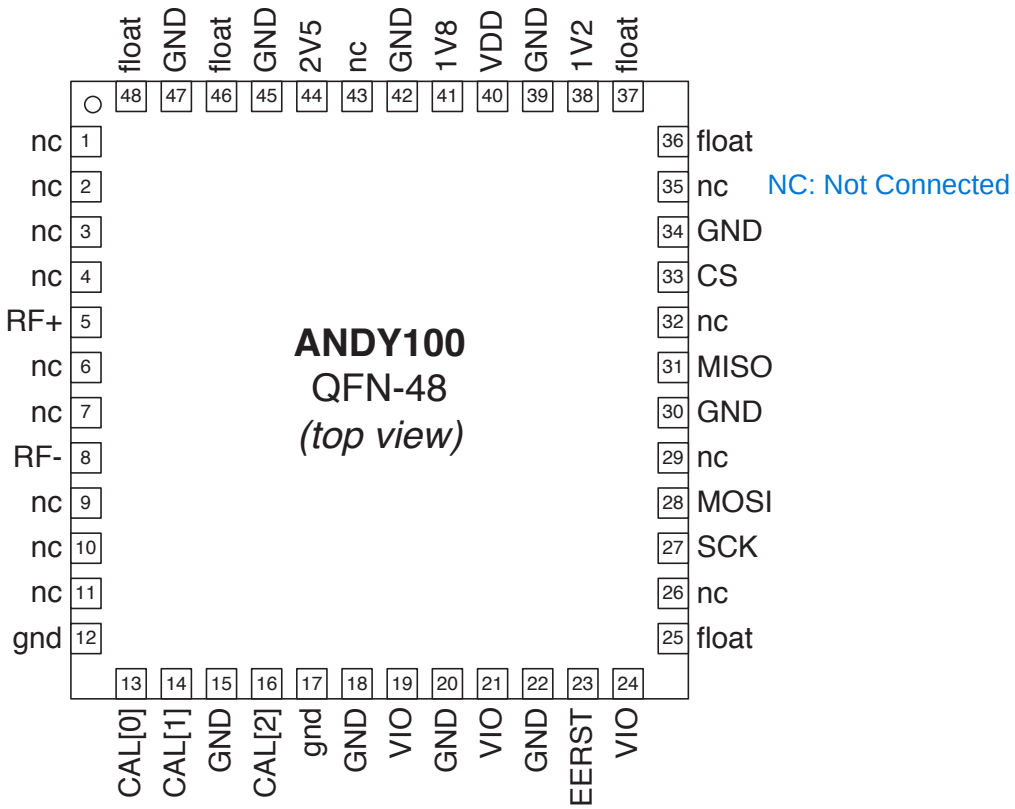


Figure 1: Pin diagram for QFN-48.

PIN		TYPE	DESCRIPTION
NAME	NO.		
RF+	5	RF	Positive input of differential RF signal.
RF-	8	RF	Negative input of differential RF signal.
VDD	40	Power	Supply voltage of the tag. This voltage is generated with the energy harvested from the RF signal of a UHF RFID reader.
2V5	44	Power	Regulated voltage output at 2.5V.
1V8	41	Power	Regulated voltage output at 1.8V.
1V2	38	Power	Regulated voltage output at 1.2V.
GND	15, 18, 20, 22, 30, 34, 39, 42, 45, 47	Power	Common ground of the generated power supplies.
VIO	19, 21, 24	Power	Power supply for the digital IOs. A voltage has to be applied to this pin externally.
CAL[0]	13	Input	Clock calibration pin 0.
CAL[1]	14	Input	Clock calibration pin 1.
CAL[2]	16	Input	Clock calibration pin 2.
CS	33	Output	SPI communication chip select line.
SCK	27	Output	SPI communication clock line.
MOSI	28	Output	SPI communication master output line.
MISO	31	Input	SPI communication master input line.
EERST	23	Input	EEPROM reset.
nc	1, 2, 3, 4, 6, 7, 9, 10, 11, 26, 29, 32, 35, 43		Internally not connected.
gnd	12, 17		Connect to GND for correct operation.
float	25, 36, 37, 46, 48		Leave unconnected for correct operation.

SOIC14

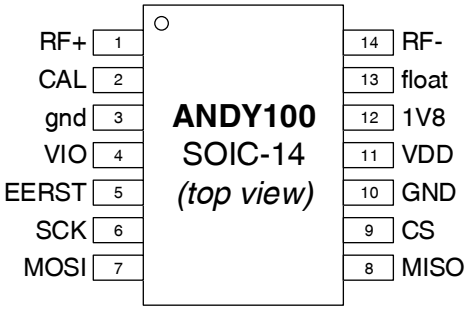


Figure 2: Pin diagram for SOIC-14.

PIN		TYPE	DESCRIPTION
NAME	NO.		
RF+	1	RF	Positive input of differential RF signal.
RF-	14	RF	Negative input of differential RF signal.
VDD	11	Power	Supply voltage of the tag. This voltage is generated with the energy harvested from the RF signal of a UHF RFID reader.
1V8	12	Power	Regulated voltage output at 1.8V.
GND	10	Power	Common ground of the generated power supplies.
VIO	4	Power	Power supply for the digital IOs. A voltage has to be applied to this pin externally.
CAL	2	Input	Clock calibration (internally connected to all trimming pins).
CS	9	Output	SPI communication chip select line.
SCK	6	Output	SPI communication clock line.
MOSI	7	Output	SPI communication master output line.
MISO	8	Input	SPI communication master input line.
EERST	5	Input	EEPROM reset.
gnd	3		Connect to GND for correct operation.
float	13		Leave unconnected for correct operation.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNIT
P_{RF}	RF input power		20	dBm
VDD	Supply voltage	-0.5	5.0	V
VIO	IO supply voltage	-0.5	5.0	V
v_{io}	Input voltage at any digital pin	-0.5	*VIO*+0.5	V
ESD	Static discharge HBM		4000	V
	Static discharge MM		200	V
$T_{storage}$	Storage temperature	-40	125	°C
$T_{operation}$	Operation temperature	-40	85	°C

This device has built-in protection against high static voltages or electric fields. However, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
RF					
RF_{SENS}	RF sensitivity	-4	-2	0	dBm
Z_{IN}	Imput impedance				
	QFN48@868MHz		8 - 67j		Ω
	QFN48@915MHz		8 - 61j		Ω
	SOIC14@868MHz		10 - 58j		Ω
	SOIC14@915MHz		10 - 53j		Ω
POWER SUPPLY					
VDD	Supply voltage	2.5	V_L	V_L+0.2	V
V_L	Limitation voltage	2.8	3.3	3.6	V
I_{DD}	Supply current when battery assited	10	15	20	μA
VIO	IO supply voltage	1.8		3.6	V
$2V5$	Regulated 2.5V output	2.25	2.5	2.75	V
I_{2V5}	Driving strength of 2V5 [1]			1	mA
$1V8$	Regulated 1.8V output	1.62	1.8	1.98	V
I_{1V8}	Driving strength of 1V8 [1]			100	μA
$1V2$	Regulated 1.2V output	1.08	1.2	1.32	V
I_{1V2}	Driving strength of 1V2 [1]			100	μA
DIGITAL IO					
V_{ih}	Input high voltage	0.7$\times VIO$		VIO+0.5	V
V_{il}	Input low voltage	-0.5		0.3$\times VIO$	V
I_{lkg}	Input leakage current			$\pm$1	μA
V_{oh}	Output high voltage	0.8$\times VIO$			V
V_{ol}	Output low voltage			0.2$\times VIO$	V
I_{drive}	Output driving strength [1]			1	mA

[1] The IC supports up to the specified driving strength. Nevertheless, if the available harvested power is insufficient, the driving strength will be limited to the available power.

NON VOLATILE MEMORY

These characteristics apply only to the physical non volatile memory included in the IC. They do not apply to the SPI memory space.

PARAMETER		MIN	UNIT
Data retention		10	years
Number of erase/write cycles	@25°C	10^5	cycles
	@85°C	10^4	cycles

MEMORY SPACE DEFINITION

The EPC Class-1 Generation-2 protocol defines a unique memory space divided in four banks: Reserved memory, EPC memory, TID memory and User memory. However, unlike traditional tags, this IC includes three different physical devices which have to be addressed from the reader. Thus, a memory map table has been defined in order to be able to access any of the physical devices from the unique memory space defined in the communication standard.

Figure 3 shows the generic structure used to map the EPC C1G2 memory space to the different devices included in the IC. As the Reserved, EPC and TID memory banks have to follow a standard-defined structure for its contents, the User memory bank is used to access the additional resources of the tag.

Some adresses of the User memory are mapped to the non volatile EEPROM, some others are reserved and the remaining are mapped to the SPI master.

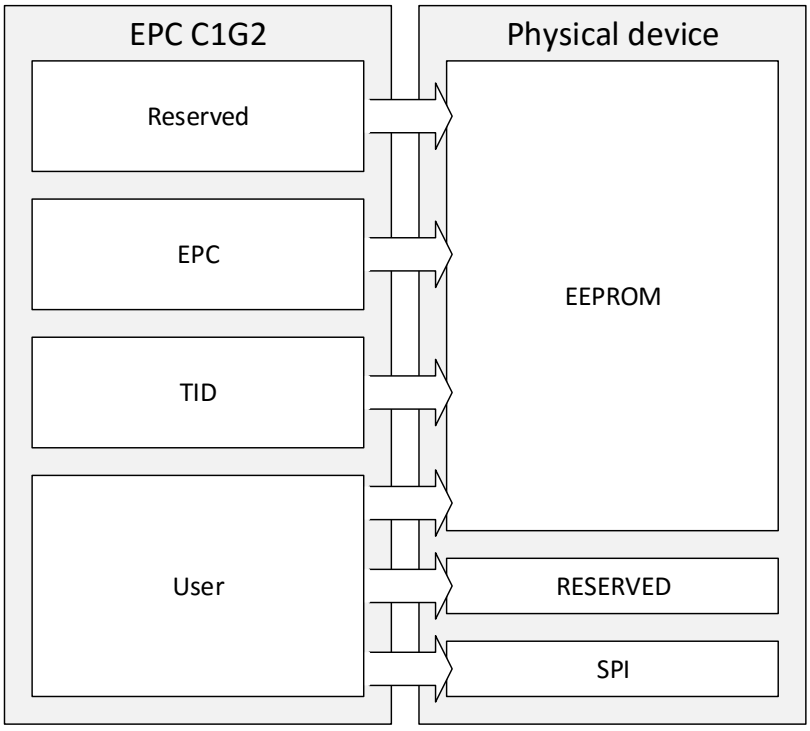


Figure 3: Memory space definition.

The memory map of the internal registers is shown in table 1. Although the only memory space exposed to the end user is the one defined in the EPC C1G2 standard, this memory space is divided in four banks. Thus the addressing of the registers consits on a memory bank identifier plus the physical address inside this memory bank. --> Add: Mem_Bank_Id + Address inside the Mem_Bank

A detailed description of each register can be found in the following section.

Table 1: Memory map.

ADDRESS	REGISTER	DESCRIPTION
RESERVED *memory bank*		
0x00	KILL_PWD_H	Kill password 16 MSB.
0x01	KILL_PWD_L	Kill password 16 LSB.
0x02	ACCESS_PWD_H	Access password 16 MSB.
0x03	ACCESS_PWD_L	Access password 16 LSB.
EPC *memory bank*		
0x00	RND_SEED	Seed for pseudo-random number generator.
0x01	STORED_PC	Protocol-control word.
0x02	EPC_5	Word 5 (MSB) of the EPC.
0x03	EPC_4	Word 4 of the EPC.
0x04	EPC_3	Word 3 of the EPC.
0x05	EPC_2	Word 2 of the EPC.
0x06	EPC_1	Word 1 of the EPC.
0x07	EPC_0	Word 0 (LSB) of the EPC.
TID *memory bank*		
0x00	TID_1	Word 1 (MSB) of the TID.
0x01	TID_0	Word 0 (LSB) of the TID.
USER *memory bank*		
0x00	SPI	Bridge to SPI master.
0x01	USER_DATA	User application data.
0x02	RESERVED	Reserved.
0x03 ... 0x3F	SPI	Bridge to SPI master.

8 Bytes insgesamt

16 Bytes insgesamt

4 Bytes insgesamt

256 Bytes

APPLICATION INFORMATION

INTRODUCTION

The RF pins of ANDY100 have to be connected to a matched differential antenna. In order to obtain a good performance a matching network has to be included to adapt the impedance of the antenna to the impedance of the tag. It is possible to avoid additional matching components if a custom antena design with matched impedance is used. More information about impedance matching and matched antenna reference designs can be found in the application note *Antenna matching for ANDY100*.

With no more external components, the IC will act as a standard identification tag responding to standard EPC C1G2 readers with its TID and EPC. In order to operate with external sensors, some considerations have to be taken into account. The first one is to ensure that the average current consumption of the sensor is in the order of several μA. For current consumptions beyond 10μA, the maximum communication distance of the system decreases.

Moreover, depending on the power consumption profile of the sensor, additional circuitry may be required. Some sensors have a high power consumption during the startup of the device. This may cause oscilation in the startup process of ANDY100. In order to prevent this behavior, an external startup circuitry has to be included in the design to keep the sensor shut down during the start up of ANDY100.

Additionally, even if the average power consumption of the sensor is low, the peak current consumption during measurement has to be evaluated. In order to support high current peaks, an external capacitor has to be included in VDD of ANDY100. The application note *External capacitor on VDD of ANDY100* discusses the best solution for including such a capacitor and the effects in the behavior of the tag.

Once the ANDY100 has been connected to a matched antenna and to a sensor with the required circuitry, a reader may singulate the tag and ask for the data contained in registers mapped to the SPI master. The tag then executes SPI communication and includes the data retrieved from the sensor in the answer backscattered towards the reader.

REGISTER DESCRIPTION

KILL_PWD_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KILL_PWD_H															

Memory bank:	Reserved
Address:	0h
Type:	R/W
Factory value:	0x0000
Description:	Kill password 16 MSB.

The KILL_PWD_H and KILL_PWD_L words compose the *Kill password* of the EPC Class-1 Generation-2 tag. The MSB of the password are stored in KILL_PWD_H, whereas the LSB are stored in KILL_PWD_L.

KILL_PWD_L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KILL_PWD_L															

Memory bank:	Reserved
Address:	1h
Type:	R/W
Factory value:	0x0000
Description:	Kill password 16 LSB.

ACCESS_PWD_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCESS_PWD_H															

Memory bank:	Reserved
Address:	2h
Type:	R/W
Factory value:	0x0000
Description:	Access password 16 MSB.

The ACCESS_PWD_H and ACCESS_PWD_L words compose the *Access password* of the EPC Class-1 Generation-2 tag. The MSB of the password are stored in ACCESS_PWD_H, whereas the LSB are stored in ACCESS_PWD_L.

ACCESS_PWD_L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCESS_PWD_L															

Memory bank:	Reserved
Address:	3h
Type:	R/W
Factory value:	0x0000
Description:	Access password 16 LSB.

RND_SEED

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RND_SEED															

Memory bank: EPC

Address: 0h

Type: R/W

Factory value: 16-bit random number.

Description: Seed for pseudo-random number generator.

The tag includes a pseudo-random number generator for the anticollision protocol. In order to obtain different number sequences among different tags, it is necessary to give diferent seeds to each tag. During the power-up process, the tag reads the value of RND_SEED and charges the pseudo-random number generator with its value. The randomness of the power-up time of the tags helps to improve the strength of the anticollision algorithm. However it is higly recommended to use different seeds.

By default, the tags are provided with random 16bit numbers programmed in the RND_SEED register.

STORED_PC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC length					**UMI**	**XI**	**NSI**								

Memory bank: EPC

Address: 1h 2h

Type: R/W

Factory value: 0x3100

Description: Protocol-control word.

[15-11] **EPC length:** The length of the EPC, in words.

[10] **UMI:** User memory indicator.

[9] **XI:** XPC_W1 indicator.

[8-0] **NSI:** Numbering system identifier.

EPC_5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_5															

Memory bank: EPC

Address: 2h

Type: R/W

Factory value: Unique EPC value.

Description: Word 5 (MSB) of the EPC.

The EPC_5, EPC_4, EPC_3, EPC_2, EPC_1 and EPC_0 words compose the *Electronic Product Code* (EPC) of the EPC Class-1 Generation-2 tag. The MSB of the EPC are stored in EPC_5, whereas the LSB are stored in EPC_0.

EPC_4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_4															

Memory bank: EPC

Address: 3h

Type: R/W

Factory value: Unique EPC value.

Description: Word 4 of the EPC.

EPC_3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_3															

Memory bank: EPC

Address: 4h

Type: R/W

Factory value: Unique EPC value.

Description: Word 3 of the EPC.

EPC_2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_2															

Memory bank: EPC

Address: 5h

Type: R/W

Factory value: Unique EPC value.

Description: Word 2 of the EPC.

EPC_1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_1															

Memory bank: EPC

Address: 6h

Type: R/W

Factory value: Unique EPC value.

Description: Word 1 of the EPC.

EPC_0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_0															

Memory bank: EPC

Address: 7h

Type: R/W

Factory value: Unique EPC value.

Description: Word 0 (LSB) of the EPC.

TID_1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TID_1															

Memory bank:	TID
Address:	0h
Type:	R/W
Factory value:	0x0000
Description:	Word 1 (MSB) of the TID.

The TID_1 and TID_0 words compose the *Tag IDentifier* (TID) of the EPC Class-1 Generation-2 tag. The MSB of the TID are stored in TID_1, whereas the LSB are stored in TID_0.

TID_0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TID_0															

Memory bank:	TID
Address:	1h
Type:	R/W
Factory value:	0x0000
Description:	Word 0 (MSB) of the TID.

USER_DATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_DATA															

Memory bank:	User
Address:	1h
Type:	R/W
Factory value:	0x0000
Description:	User application data.

SPI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI															

Memory bank:	User
Address:	[0h, 3h-3Fh]
Type:	R/W
Description:	Bridge to SPI master.

SPI OPERATION

ANDY100 includes specific hardware for master SPI operation. This hardware uses the SPI configuration CPOL=1 and CPHA=1, which is commonly known as mode 3. The serial interface interacts with SPI slaves with 4 wires: CS, SCK, MOSI and MISO.

CS is the Chip Select signal which enables the slave device. The master drives this signal low at the start of the communication and drives it back high at the end.

SCK is the serial clock and it is driven by the SPI master. In mode 3 the idle state of the SCK line is high.

MOSI and MISO are respectively the Master Output Slave Input data port and the Master Input Slave Output data port. These lines are driven at the falling edge of SCK and should be captured at the rising edge of SCK. MOSI is driven by the master whereas MISO is driven by the slave. After a succesful communication, the master drives the MOSI signal high into the idle state.

The SPI master includes fixed read register and write register commands. Both of them are completed in 16 clock pulses or in multiple of 8 in case of multiple bytes read. Bit duration is the time between two falling edges of SCK. The first bit (bit 0) starts at the first falling edge of SCK after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SCK just before the rising edge of CS.

Command structure

ANDY100 can perform read register and write register operations. Both of them can be used to perform a single register access or multiple register access. The command structure in the SPI interface is shown in figure 4.

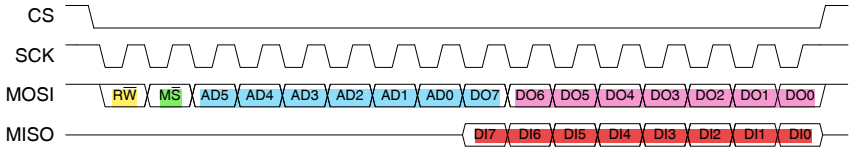


Figure 4: SPI command timing diagram.

bit 0: RW bit. When 0, the data DO(7:0) is written into the slave device. When 1, the data DI(7:0) from the slave device is read.

bit 1: MS bit. When a multiple read operation is requested, this bit is set to 1. The slave device should increment the register address automatically every 8 cycles of SCK.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (write mode). This is the data that is written into the device (MSb first).

bit 8-15: data DI(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read commands further blocks of 8 clock periods will be added.

When a read or write operation is commanded from the EPC C1G2 interface pointing to a memory address mapped to the SPI bridge, the corresponding signaling is generated in the SPI interface. If a single word read is requested from the EPC C1G2 side, a single register read will be executed. If several words are requested within the same EPC C1G2 read command, a multiple register read will be executed. If a word write is requested from the EPC C1G2 interface, a single register write will be executed in the SPI interface.

The address used in the adress bits of the SPI signaling is the address of the register inside the User bank of the EPC C1G2 memory space. The values of RW and MS are set depending on the requested operation.

Read command

Figure 5 shows the timing diagram of the SPI signaling executed upon the reception of a EPC C1G2 read command containing a single word mapped to the SPI bridge.

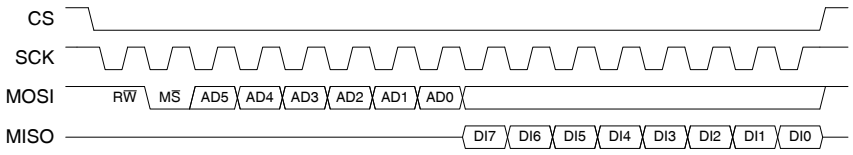


Figure 5: SPI single read timing diagram.

Figure 6 shows the timing diagram of the SPI signaling executed upon the reception of an EPC C1G2 read command containing two words mapped to the SPI bridge. If more words are requested in the read command, the SPI master will issue more SCK cycles until all the SPI registers have been read.

The SPI master included in ANDY100 can execute multiple register read commands of up to 6 registers. If more than 6 registers have to be read, this has to be done issuing separate read commands.

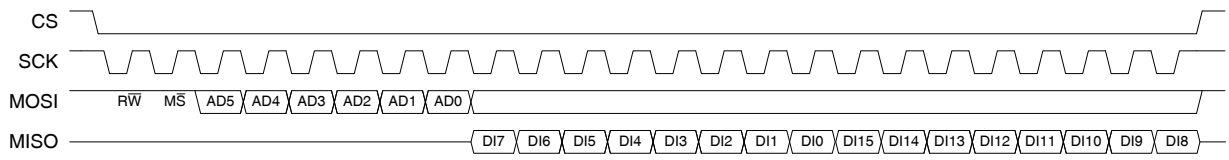


Figure 6: SPI multiple read timing diagram.

In the response to EPC C1G2 read commands, ANDY100 includes the data that has been read in the MISO line during the SPI communication. The register word length used in the SPI interface is 8 bits whereas the length of the EPC words is 16 bits. The data of the SPI register word is right aligned inside the word of the EPC register in the answer to the reader. Thus, all the data read from the SPI bridge will contain 8 initial 0's followed by the value of the SPI register in each word.

Write command

Figure 7 shows the timing diagram of the SPI signaling executed upon the reception of a EPC C1G2 write command addressed to a word mapped to the SPI bridge.

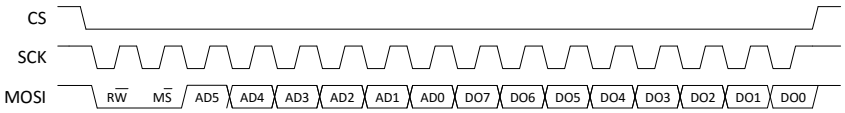


Figure 7: SPI write timing diagram.

As for the read command, the word length conversion between EPC C1G2 and SPI memory spaces is done by right aligning the 8 bit SPI word inside the 16 bit EPC C1G2 word.

APPLICATION EXAMPLES

Figure 8 shows the basic block diagram of the KINEO-A3DH battery free orientation sensor tag. This design includes a LIS3DH accelerometer of STMicroelectronics, which is directly compatible with the SPI interface of the ANDY100. For more information check the website.

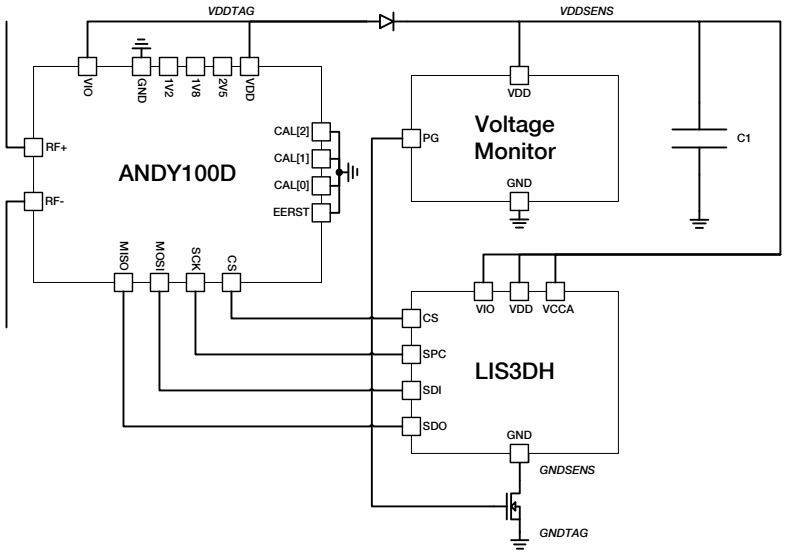


Figure 8: KINEO orientation sensor with LIS3DH.

Figure 9 shows the basic block diagram of the PYROS-03GC battery free contact temperature sensor tag. This design includes a thermistor, an analog signal conditioning circuitry and a micro-controller with integrated ADC. For more information check the website.

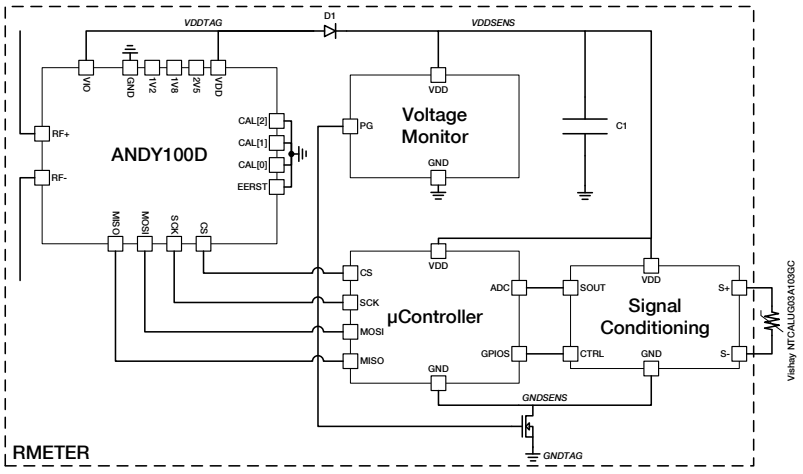


Figure 9: PYROS-03GC contact temperature sensor with NTC thermistor.

Figure 10 shows the basic block diagram of the STELLA-LEDW703 battery free LED indicator tag. This design includes an LED and a micro-controller. For more information check the website.

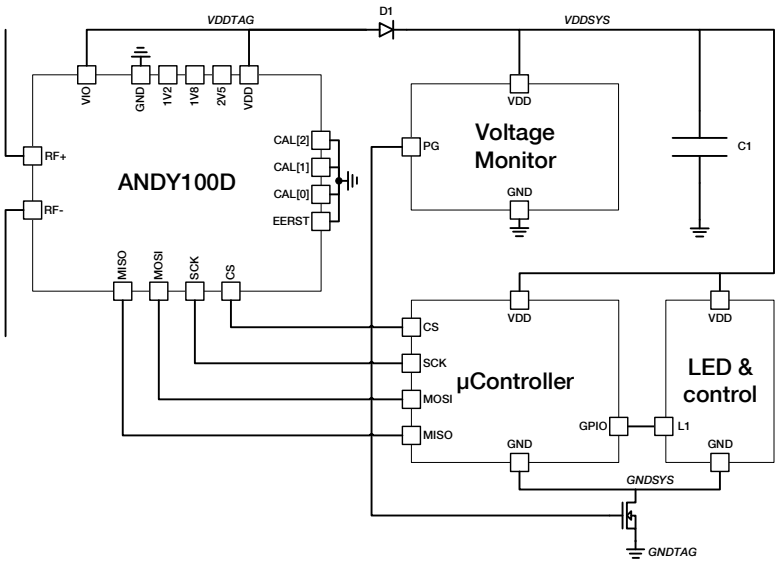


Figure 10: STELLA-LEDW703 LED indicator.

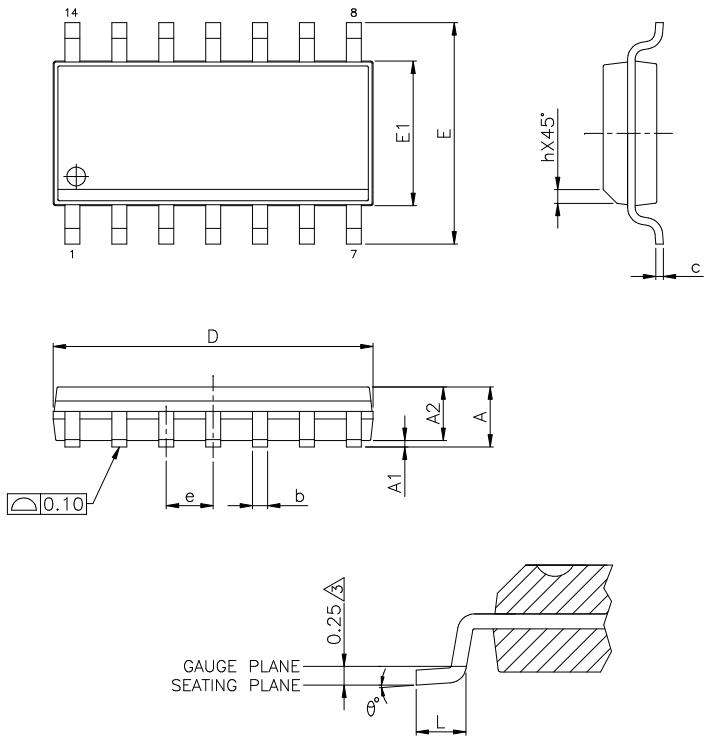
REFERENCES

The next table shows the available references of the ANDY100.

Ref.	Name	Status(1)	Package
01014	ANDY100-S14-D	ACTIVE	SC14
01015	ANDY100-S14-U	ACTIVE	SC14
01048	ANDY100-Q48-D	NRND	QF48
01049	ANDY100-Q48-U	NRND	QF48

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: Farsens has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but Farsens does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: Farsens has discontinued the production of the device.

PACKAGE DESCRIPTION (SC14)



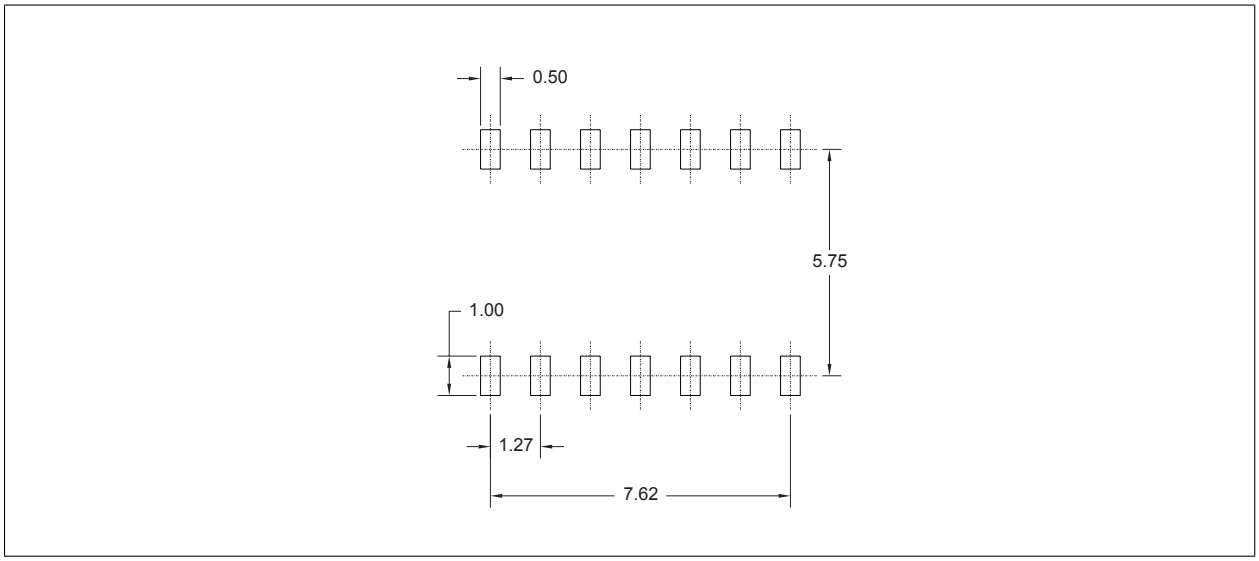
SYMBOLS	MIN.	MAX.
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.10	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

UNIT : mm

NOTES:
1.JEDEC OUTLINE : MS-012 AB REV.F
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

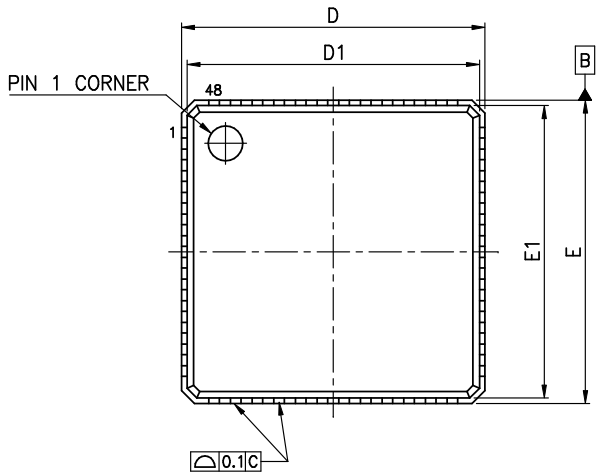
Notes: 1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

RECOMMENDED LAND PATTERN (SC14)



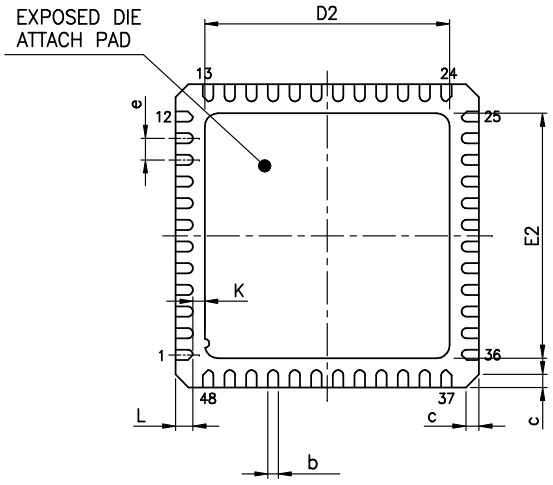
Notes: 1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

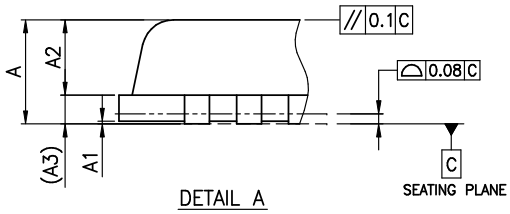
PACKAGE DESCRIPTION (QF48)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	6.90	7.00	7.10
D1	6.65	6.75	6.85
E	6.90	7.00	7.10
E1	6.65	6.75	6.85
e		0.50 BSC.	
K	0.20	—	—
L	0.30	0.40	0.50
θ°	0.00	—	12.00
D2	5.68	5.75	5.80
E2	5.68	5.75	5.80

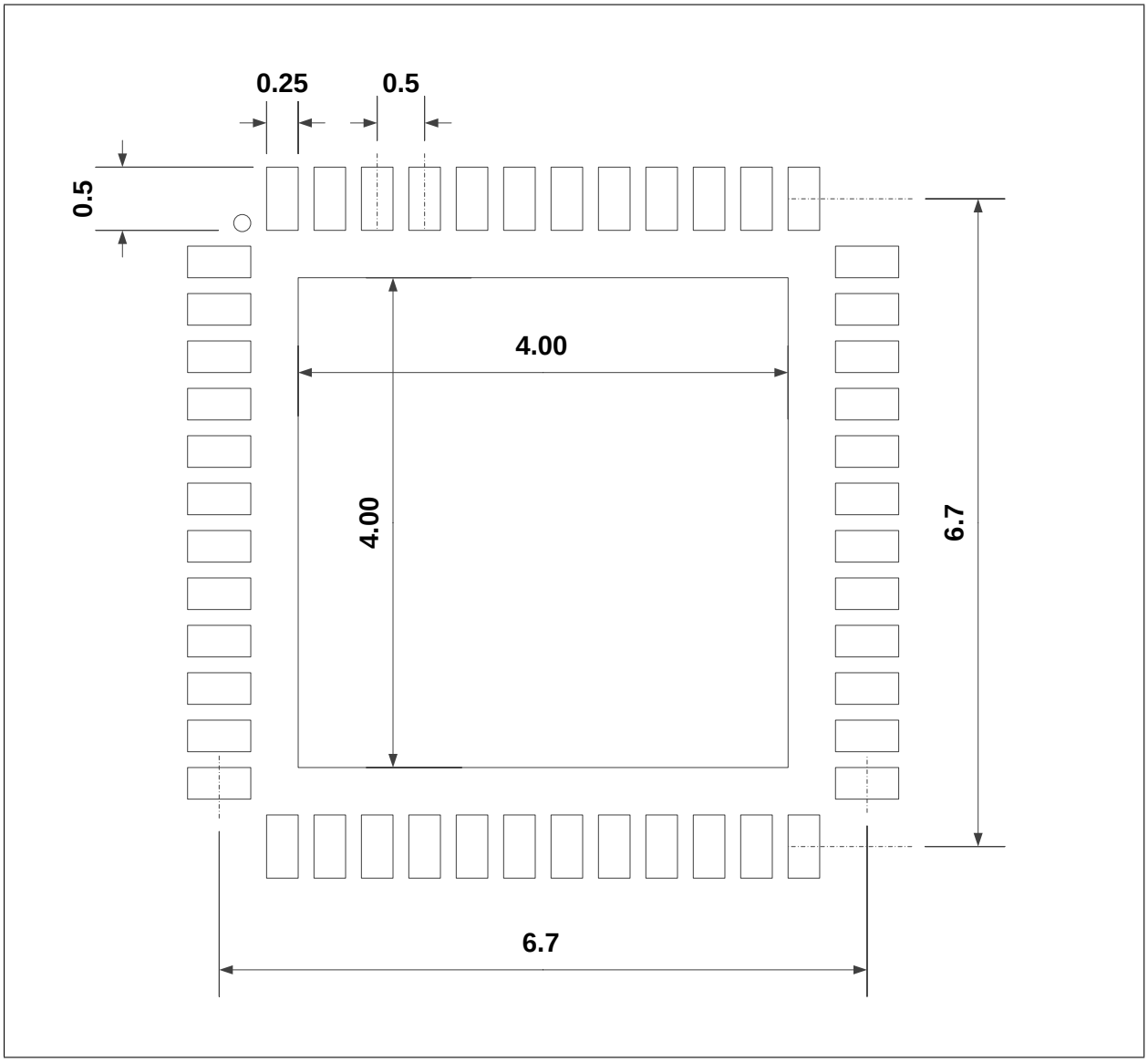
UNIT : mm





Notes: 1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

RECOMMENDED LAND PATTERN (QF48)



Notes: 1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.