Application note
L9916 OTP Programming
Rel. 1.2 – Oct 20th 2016

Introduction

L9916 is a monolithic multifunction voltage alternator for 12V and 24V systems.
The device includes an OTP (One Time Programmable) memory to store factory configuration parameters.
Purpose of this document is to explain how to program and test the OTP block.

OTP parameters

OPT parameters are organized in 6 pairs of 8-bit registers (or rows) identified through a row-number from 0 to 5. Register pairs (column 0 and column 1) has been introduced to increase data reliability.

The following tables show OTP rows content: parameters' description is out of the scope of this document.

OTP Row 0

Table 1 - Row 0

Bit	Description	
D7 : D4	PIN B+ : Set Point Voltage selection (12V | 24V)	0000 = 14.5V | 29.0V (default) 0001 = 14.6V | 29.2V 0010 = 14.3V | 28.6V 0011 = 14.4V | 28.8V 0100 = 14.9V | 29.8V 0101 = 15.0V | 30.0V 0110 = 14.7V | 29.4V 0111 = 14.8V | 29.6V 1000 = 13.7V | 27.4V 1001 = 13.8V | 27.6V 1010 = 13.5V | 27.0V 1011 = 13.6V | 27.2V 1100 = 14.1V | 28.2V 1101 = 14.2V | 28.4V 1110 = 13.9V | 27.8V 1111 = 14.0V | 28.0V
D3	Pin B+ : activate Set Point Voltage clamp at low temperature	0 = disabled (default) 1 = enabled
D2 : D0	Pin B+ : Thermal compensation	000 = -10 mV/°C (default) 001 = -7 mV/°C 010 = -3.5 mV/°C 011 = -2.0 mV/°C 1xx = 0 mV/°C

OTP Row 1

Table 2 - Row 1		
Bit	Description	
D7	Pin B+ : 12V selection (default 24V)	0 = 24V (default) 1 = 12V
D6	Pin B+ : regulated voltage variation with load (12V | 24V)	0 = 300mV | 400mV (default) 1 = 200mV | 300mV
D5	Reserved	
D4	Reserved	
D3	SDT enable	0 = enabled (default) 1 = disabled
D2	Pin Sense: Select whether to turn on the Lamp in case of SENSE loss	0 = lamp OFF (default) 1 = lamp ON
D1	Pin Sense: Disable Vsetpoint +1V in case of SENSE loss	0 = Vsetpoint + 1V (default) 1 = Vsetpoint
D0	Pin Sense: select the SENSE difference between B+ and SENSE	0 = 1.6V (default) 1 = 2.3V

OTP Row 2

Table 3 - Rows 2		
Bit	Description	
D7 : D6	Pin F: Field frequency	00 = 125 Hz (default) 01 = 250 Hz 10 = 333 Hz 11 = 400 Hz
D5	Pin F: LRC disable	0 = LRC enabled (default) 1 = LRC disabled
D4 : D2	Pin F: LRC time selection	000 = 2.5 s (default) 001 = 5 s 010 = 7.5 s 011 = 10 s 100 = 3 s 101 = 6 s 110 = 9 s 111 = 12 s
D1 : D0	Pin F: Start Delay Time selection	00 = 0.5 s (default) 01 = 2.5 s 10 = 5 s 11 = 10 s

OTP Row 3

Table 4 - Row 3		
Bit	Description	
D7 : D6	Pin PH: poles number	00 = 6 Pole pairs (default) 01 = 7 Pole pairs 10 = 8 Pole pairs 11 = 8 Pole pairs
D5 : D4	Pin PH: speed to exit pre-excitation	00 = 1200 rpm (default) 01 = 900 rpm 10 = 1800 rpm 11 = 1500 rpm
D3 : D2	Pin PH: speed for self-start operation	00 = 2800 rpm (default) 01 = 3200 rpm 10 = 1200 rpm 11 = 1500 rpm
D1 : D0	Pin PH: speed to exit/enter LRC operation (LRC cut)	00 = 3200 rpm (default) 01 = 3000 rpm 10 = 2800 rpm 11 = 1500 rpm

OTP Row 4

Table 5 - Row 4		
Bit	Description	
D7 : D6	Pin PH: select self-start phase voltage threshold (VP_{HTh_SS1} - $VP_{LTh\_\_SS1}$)	00 = 0.37V – 0.24V (default) 01 = 0.76V – 0.45V 10 = 1.22V – 0.98V 11 = 1.45V – 0.98V
D5	Pin PH: select LRC always active	0 = LRC always active disabled (default) 1 = LRC always active enabled
D4	Pin B+ : 12V selection (default 24V)	0 = 24V (default) 1 = 12V
D3	Pin PH: select self-start function	0 = enabled (default) 1 = disable
D2	Pin IGN: mode select	0 = Mode 1 (default) 1 = Mode 2
D1	Pin IGN: enable	0 = IGN disabled (default) 1 = IGN enabled
D0	Pin IGN: select whether in case of IGN open the LAMP must turn-on	0 = lamp OFF (default) 1 = lamp ON

OTP Row 5

Table 6 - Row 5		
Bit	Description	
D7	OTP write protection	0 = not protected (default) 1 = protected
D6	Pin FM: behavior in comparison with F signal	0 = reverse (default) 1 = not reverse
D5	Pin FM: duty cycle clamp	0 = not active (default) 1 = active
D4	Pin FM: frequency in comparison with F signal	0 = F frequency (default) 1 = F frequency/2
D3	Pin B+ : 12V selection (default 24V)	0 = 24V (default) 1 = 12V
D2 : D1	Pin L: alarm validation time	00 = 0.5 s 01 = 1 s 10 = 1.5 s 11 = 2 s
D0	Pin L: disable high side when lamp is OFF	0 = no (default) 1 = yes

Duplicated fields

For safety reasons 12V selection field has 6 copies that need to be programmed: the final selection is computed as follows:

Final 12 V Sel = ($12V\_D7_{row1/col0}$ OR $12V\_D7_{row1/col1}$) AND
($12V\_D4_{row4/col0}$ OR $12V\_D4_{row4/col1}$) AND
($12V\_D3_{row5/col0}$ OR $12V\_D3_{row5/col1}$)

Programming OTP bits

A not-programmed OTP contains all 0s; programming a bit means changing its status from 0 to 1. Once programmed the original status cannot be restored.
OTP bits programming logic is the following:

Table 7 – OTP status change			
Value to Program	Previous bit status	Status after program	
0	0	0	The program operation is ignored
1	0	1	The program operation is effectively executed
0	1	1	The program operation is ignored
0	1	1	The program operation is ignored

OTP Program sequence

To program an OTP cell it is necessary to implement the following sequence:

Table 8 – OTP program sequence	
Step	Status after program
1	Prepare OTP program setup (data and address)
2	Send OTP write command
3	Wait for end-of-busy
4	Send OTP write command
5	Wait for end-of-busy
6	Send OTP write command
7	Wait for end-of-busy

Due to the internal architecture a program command has to be sent three times.

It is important to outline that a just written OTP row is not available to the system until it is reloaded through an OTP read operation.

OTP redundancy

As already mentioned all OTP rows are duplicated into two columns (column 0 and column 1); there isn't any column selection logic or any column check logic: bit-fields of the two columns are logically OR-ed and the used by the device.

For example SDT enable bit (but 3 of row 1) will be used by the internal logic as shown in the following table:

Table 9 – OTP redundancy		
Column 0/Row1/Bit3	Column 1/Row1/Bit3	Effective SDT enable
0	0	0
0	1	1
1	0	1
1	1	1

OTP protection

OTP write operation can be inhibited by setting bit 7 of row 5 in one or both columns as shown in the following table:

Table 10 – OTP protection		
Column 0/Row5/Bit7	Column 1/Row5/Bit7	OTP status
0	0	Not protected
0	1	Protected
1	0	Protected
1	1	Protected

OTP protection effectiveness

OTP protection is effective only when at least one copy of ROW 5 is read: in this case the protection flag is transferred from the OTP to the internal logic that is in charge to handle protection strategy.

A protection operation composed by protection bit write followed by the relevant read has the following effects:

- Any OTP write operation is inhibited
- Any OTP read operation is inhibited until next power-on

For this reason, when writing OTP protection bits (rows 5/0 and 5/1) avoid to read the row immediately after the OTP write because the second write will not be executed; the suggested sequence is:

Table 11 – OTP protection strategy		
Step	Operation	Note
X	Write any row and, if needed, check the value with the relevant read operation	
X + 1	Write all desired bit to row 5/0 with protection bit set	OTP write is performed but not yet effective
X + 2	Write all desired bit to row 5/1 with protection bit set	OTP write is performed but not yet effective
X + 3	Power off	
X + 4	Power on	
X + 5	Read and check row 5/0	
X + 6	Read and check row 5/1	

OTP protection examples

This effect can lead to some misunderstanding and the following table gives an example:

Table 12 – OTP protection example 1

Step	Operation	Note
1	Write A0 to row 2/0	
2	Read row 2/0	The read value is A0
3	Write AA to row 2/0	
4	Write 55 to row 3/0	
5	Read row 3/0	The read value is 55
6	Write 80 to row 5/0	Write a protection bit
7	Write 5F to row 3/0	Write access after an incomplete protection operation
8	Read row 5/0	The read value is 80: now the protection operation is complete
9	Read row 3/0	The read value is 55 because the written 5F value has not yet been transferred: it is present in the OTP but the transfer to the logic has been inhibited by the protection operation
10	Read row 2/0	The read value is A0 because row 2 have never been read after last OTP write operation and the protection has inhibited any data transfer
11	Power Off	
12	Power On	
13	Read row 2/0	The read value is AA because data transfer inhibition is no longer active
14	Read row 3/0	The read value is 5F because data transfer inhibition is no longer active and the last write operation was done when the protection was not yet complete

Table 13 – OTP protection example 2

Step	Operation	Note
1	Write A0 to row 2/0	
2	Read row 2/0	The read value is A0
3	Write AA to row 2/0	
4	Write 55 to row 3/0	
5	Read row 3/0	The read value is 55
6	Write 80 to row 5/0	Write a protection bit
7	Read row 5/0	The read value is 80: now the protection operation is complete
8	Write 5F to row 3/0	Write access after complete protection operation
9	Read row 3/0	The read value is 55 because the write operation was not allowed due to complete protection sequence
10	Read row 2/0	The read value is A0 because row 2 have never been read after last OTP write operation and the protection has inhibited any data transfer
11	Power Off	

12	Power On	
13	Read row 2/0	The read value is AA because data transfer inhibition is no longer active
14	Read row 3/0	The read value is 55 because OTP write attempt was done when the protection was complete

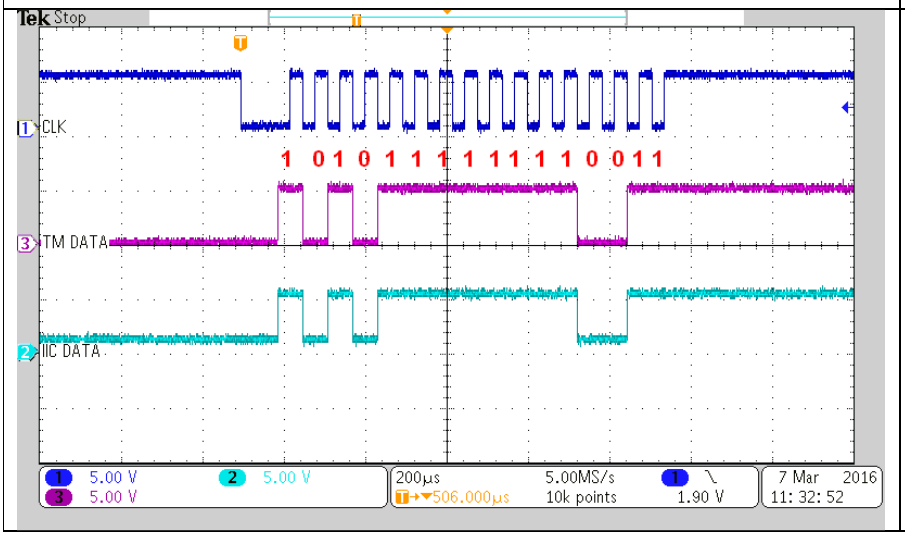
Device Program Mode

The device has no communication line and any OTP access can be done enabling the “Device Programming Mode”: in this mode IGN, PHASE and DFM pin change functions and can be used to sustain a communication protocol.

Entering Device Program Mode

Starting from Stand-By condition (internal regulators inactive), with all input terminals (IGN, PHASE and LAMP) set a 0V and battery terminal to 15.7V, to initiate the mode change procedure a fixed bit pattern [0xAFF3 = 1010111111110011b] must be applied to IGN pin synchronously with a clock signal applied to PH pin; the following snapshots shows an example:

Fig.1 – Device Program Mode entry sequence



Data are sampled on clock rising edge

After the initial sequence, within a ~500 ms interval, an I2C protocol has to be applied to pins PH (SCL – I2C clock) and DFM (SDA – I2C data) in order to confirm the “Device Program Mode”.
If the timeout elapses before the confirmation pattern has been sent the device returns to normal mode otherwise it recognizes the “Device Program Mode” waiting for commands from the communication line.

I2C communication

I2C is a 2-wires master-slave byte-oriented communication protocol, refer to the relevant literature for details. The typical I2C frame implemented on the device has the following fields:

Table 14 – I2C frame		
Field	Description	Notes
I2C address	0xD8 (11011000b): write address 0xD9 (11011001b): read address	Bit 0 is set for read commands
Sub-Address	8 bits: D7 = **I**ncrement bit set when it is intended to access to consecutive sub-addresses D6:D0 First sub-Address value	
Data		
Data		

The internal structure of the device is organized into registers: the I2C sub-address field specifies the address register to access.

I2C Write procedure

There are two possible procedures:

1. Without increment: **I** bit is set to 0 and the register to be written is addressed by the sub-address. All DATA bytes following the sub-address will be written to the same register.
2. With increment: **I** bit is set to 1 and the first register to be written is addressed by sub-address. The first DATA byte will be written to the register addressed by the sub-address field whereas the following DATA bytes (if any) will be written to incremented addresses.

I2C Read procedure

There are two possible procedures:

1. Without increment: **I** bit is set to 0 and the register to be read is addressed by the sub-address. All bytes following the sub-address will be read from the same register.
2. With increment: **I** bit is set to 1 and the first register to be read is addressed by sub-address. The first DATA byte will be read from the register addressed by the sub-address field whereas the following DATA bytes (if any) will be read from incremented addresses.

Data Validity

The data on the SDA line must be stable during the high half-period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

The start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH, the stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

I2C protocol is byte (8 bits) oriented with MSB is transferred first.

Transmitter and Receiver

Having, the I2C protocol, only one data wire, both master and slave nodes can be a transmitter and/or a receiver node:

Table 15 – I2C transmitter and receiver			
I2C write		I2C read	
Master	Transmitter	Master	Receiver
Slave	Receiver	Slave	Transmitter

All I2C frames are initiated by the master mode that has always to transmit address and sub-address fields.

After each I2C byte the transmitter node puts a resistive HIGH level on the SDA line during the acknowledge clock pulse in order to let the receiver node to pull-down the line.

I2C Registers

As already mention the Device Program Mode logic is organized into registers addressed with the I2C protocol.
I2C register has not to be confused with OTP rows mentioned in the first chapters.

Register 0x01

This register is used to confirm or to exit the Device Program Mode:

- Confirmation: to confirm the Device Program Mode the very first I2C frame after the initialization sequence has to write 0xA0 to register 1
- Exit: to exit the Device Program Mode the host has to write 0x00 to register 1 and wait for the ~500ms timeout

Register 0x09

This register is used to store the data to transfer to an OTP row/column specified through register 0x0A.

Registers 0x0A

This register is used to specify the OTP row/column to address and the type of access.

Table 16 – Register 0x0A		
Bit	Default	Description
D7	0	Reserved
D6:D5	00	00= Reserved (default) 01= Row Write (data are effectively written to OTP) 10= Row Read 11= Row Write Simulation (data are not effectively written to OTP)
D4	0	Column selection
D3:D0	0	Row selector

Register 0x0B

This clear-on-read register is used to check OTP status:

Table 17 – Register 0x0B		
Bit	Default	Description
D7	0	Reserved
D6	0	Reserved
D5	0	This bit is high during column 1 write operation
D4	0	This bit is set at the end of a column 1 write operation
D3	0	This bit is set at the end of a column 1 load operation after Power on reset (POR)
D2	0	This bit is high during column 0 write operation
D1	0	This bit is set at the end of a column 0 write operation
D0	0	This bit is set at the end of a column 0 load operation after Power on reset (POR)

Once written, data can be available and or valid according to different conditions as shown in the following table:

Table 18 – Written rows status		
	Data Validity	Data Availability
Row Write	Once written, data are permanent and always valid	Written data are not immediately available and usable by the internal logic. They will be available after one or more

		the following actions: • Data read command • Device Reset • Device Power Off and Power On sequence
Row Write Simulation	Once written, data immediately valid until they are overwritten by an OTP read operation or by a write simulation or the device is not reset or unpowered	Data are immediately available and usable by the internal logic: to use the programmed parameters in application mode it is necessary to exit the Device Program Mode without resetting or removing the power

Register 0x0C

This register contains the 8 bit value of the addressed row/column after a read access command.

OTP simulation

In order to test the device and the application without “burning” a lot of devices it is possible to simulate the write operation.
To work and exercise the device with simulated configurations bits it is necessary to proceed as follows:

1. Enter Device Program Mode
2. Write Simulated Configurations bits
3. Exit Device Program Mode without resetting or powering-off the device: it will be ready to work with simulated data after the ~500 ms timeout

Simulated data are valid until one of the following event occurs:

- Device reset
- Device power off
- **Read command: after a simulation write it is not possible to verify the data because the read operation always loads data from the real OTP overriding simulated data**

OTP access examples

OTP row write

Supposing to write the 0x5A value to OTP row 4/column 0 it is necessary to implement the following sequence:

Table 19 – OTP write sequence			
Operation	I2C register address	Value	
Write	0x09	0x5A	
Write	0x0A	0x24	Write command to row 0x04
Read Loop	0x0B		Check D2 bit and wait it is cleared
Write	0x0A	0x24	Write command to row 0x04
Read Loop	0x0B		Check D2 bit and wait it is cleared
Write	0x0A	0x24	Write command to row 0x04
Read Loop	0x0B		Check D2 bit and wait it is cleared

OTP row read

Supposing to read OTP row 2 it is necessary to implement the following sequence:

Table 20 – OTP read sequence			
Operation	I2C register address	Value	
Write	0x0B	0x42	Read command from row 0x02
Read	0x0C		Get data
Read	0x0D		Get column 0 and column 1 OR-ed data