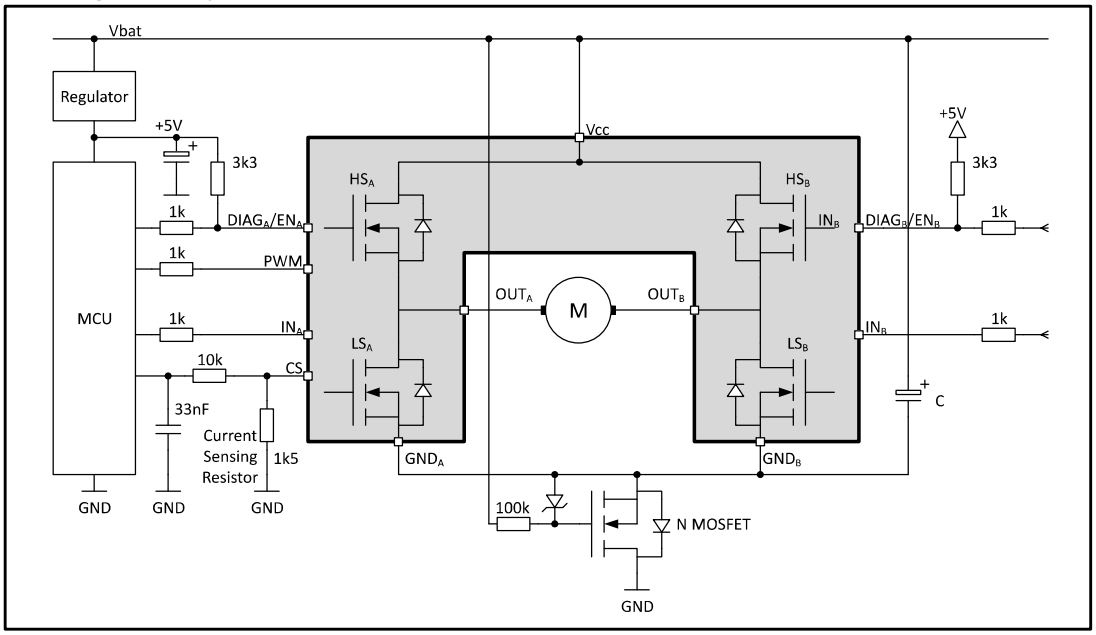
The VNH5XXX devices with PWM capability are immune to this phenomena thanks to an optimized gate charge and a suitable internal dead time.

2.3 VNH5XXX general application schematic

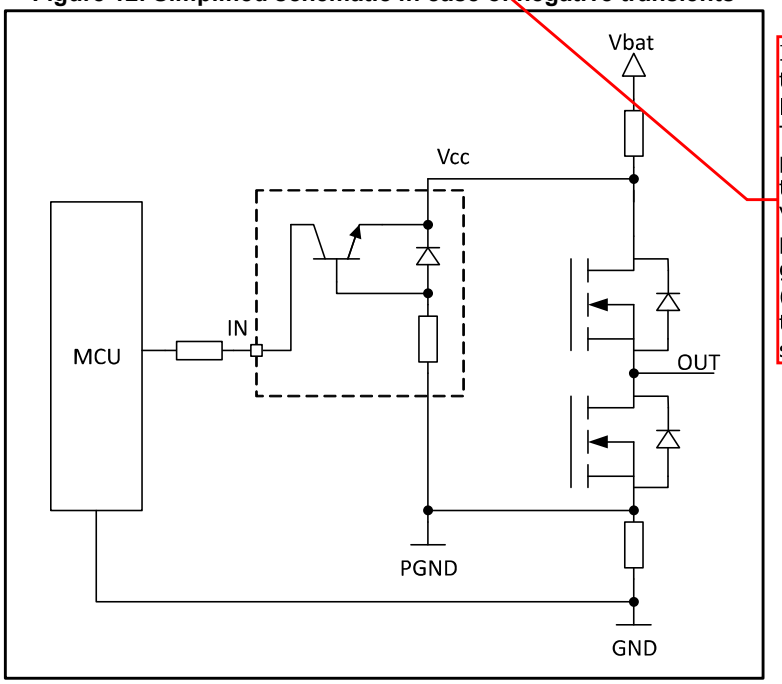
The following figure illustrates the general application scheme for device connection to the microcontroller and to enable the basic functions.

Figure 11: Typical application circuit forVNH5XXX for DC to 20 kHz PWM operation



MCU I/Os protection: When negative transients are present on the Vcc line, the control pins are pulled negative to approximately -1.5 V (2 x V_{BE}) due to the internal path from the pin to ground (the parasitic bipolar transistor goes in saturation, see the figure below).

Figure 12: Simplified schematic in case of negative transients



※Is it possible that -1.5V is applied to the CPU for all IN, PWM, DIAGx/ENx? I think the above circuit is an explanation of the parasitic transistors, not an equivalent circuit for the pins. I would like to have the equivalent circuit for each pin if possible. Does this countermeasure rely on the parasitic diode protection of the CPU? Are there any pull-down resistors in each input port?

ST suggests connecting a resistor (Rprot) between the microcontroller and the device input in order to prevent the microcontroller I/Os pins from latching-up. The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input level compatibility) with the latch-up limit of microcontroller I/Os:

$$\frac{1.5}{I_{latchup}} \leq Rprot \leq \frac{(VOH\mu C - VIH)}{I_{IHmax}}$$

ST suggests connecting a resistor (RPROT) between the microcontroller and the device input to prevent the microcontroller's I / O pins from latching up. These resistor values are a compromise between the leakage current of the microcontroller and the current required for HSD I/O (input level compatibility). Microcontroller I/O latch-up limits

Example:

- Ilatchup > 20 mA
- VOHµC > 4.5 V
- VIH= 2.1 V
- IIHmax = 10µA
- 75 Ω ≤ Rprot ≤ 240 KΩ: recommended Rprot = 1 KΩ

IN_A and IN_B: The input signals are used to select the motor direction and the brake condition. State INx =1 means the related HSx of the leg is turned on and the LSx is turned off (when INx=0, HSx is off and LSx is on). In all cases, a low level state on the signal PWM turns both the low side switches off.

PWM pin (not present in VNH5200AS) usage: The PWM pin can be driven with a frequency of up to 20 KHz. It allows controlling the speed of the motor by driving the low side drivers MOS. In all cases, a “0” on the PWM pin turns both LSA and LSB switches off. When PWM rises back to “1”, LSA or LSB turn on again depending on the states of the input signals IN_A and IN_B.

Blocking capacitor: The value of the capacitor (C) depends on the application conditions and defines voltage and current ripple on supply line at PWM operation. The stored energy of the motor inductance may fly back into the blocking capacitor if the bridge driver goes into the 3-state. This causes a hazardous overvoltage if the capacitor is not big enough. Generally, 500 µF per 10 A load current is recommended.

$DIAG_X$/EN_X: in normal operating conditions, this pin is considered as an input by the device; it must be externally pulled high. As DIAGX/ENX are set from low to high, after a power on reset delay time of 2 µs, the logic with its relevant protection is enabled.

When a fault occurs, the faulty leg of the bridge is latched off and the corresponding $DIAG_X$/EN_x pin is pulled low to indicate the fault. To turn on the respective output (OUT_x) again, the input signal must rise from low to high level (see *Section 4.5.2: "Unlatching of VNH5XX bridges"*).

CS_DIS (not present in VNH5200AS): a logic level high on CS_DIS pin sets the current sense pins of the device to a high-impedance state, thus disabling current monitoring. This feature allows the multiplexing of the microcontroller analog inputs by sharing the sense resistance and the ADC line among different devices.

2.4 VN577X features

VN5770AKP and VN5772AK, featuring an R_{on} of 280 mΩ and 100 mΩ per leg respectively, are two devices made up of three independent monolithic chips housed in a standard SO-28 package. The devices are suitable to drive a DC motor in a bridge configuration or used as a quad switch for any low-voltage application.

The double high-side integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart. An analog current sense (CS) pin delivers a current proportional to the load current (according to a known ratio) and indicates overtemperature shutdown of