

STM32 CubeMX

1. Description

1.1. Project

Project Name	MOUNIA
Board Name	custom
Generated with:	STM32CubeMX 6.11.1
Date	05/19/2024

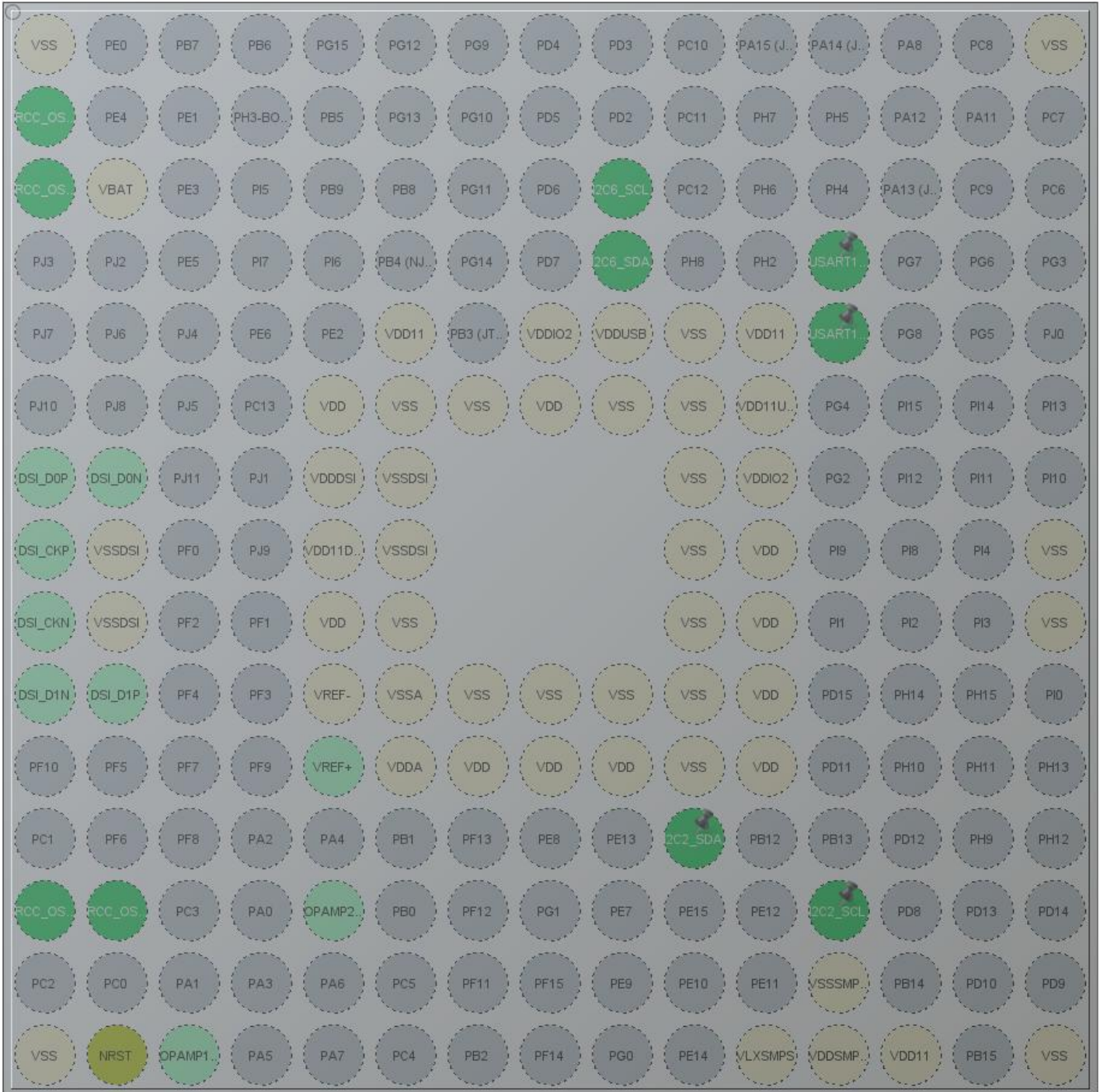
1.2. MCU

MCU Series	STM32U5
MCU Line	STM32U599/5A9
MCU name	STM32U5A9NJHxQ
MCU Package	TFBGA216
MCU Pin number	216

1.3. Core(s) information

Core(s)	ARM Cortex-M33
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2. Pinout Configuration



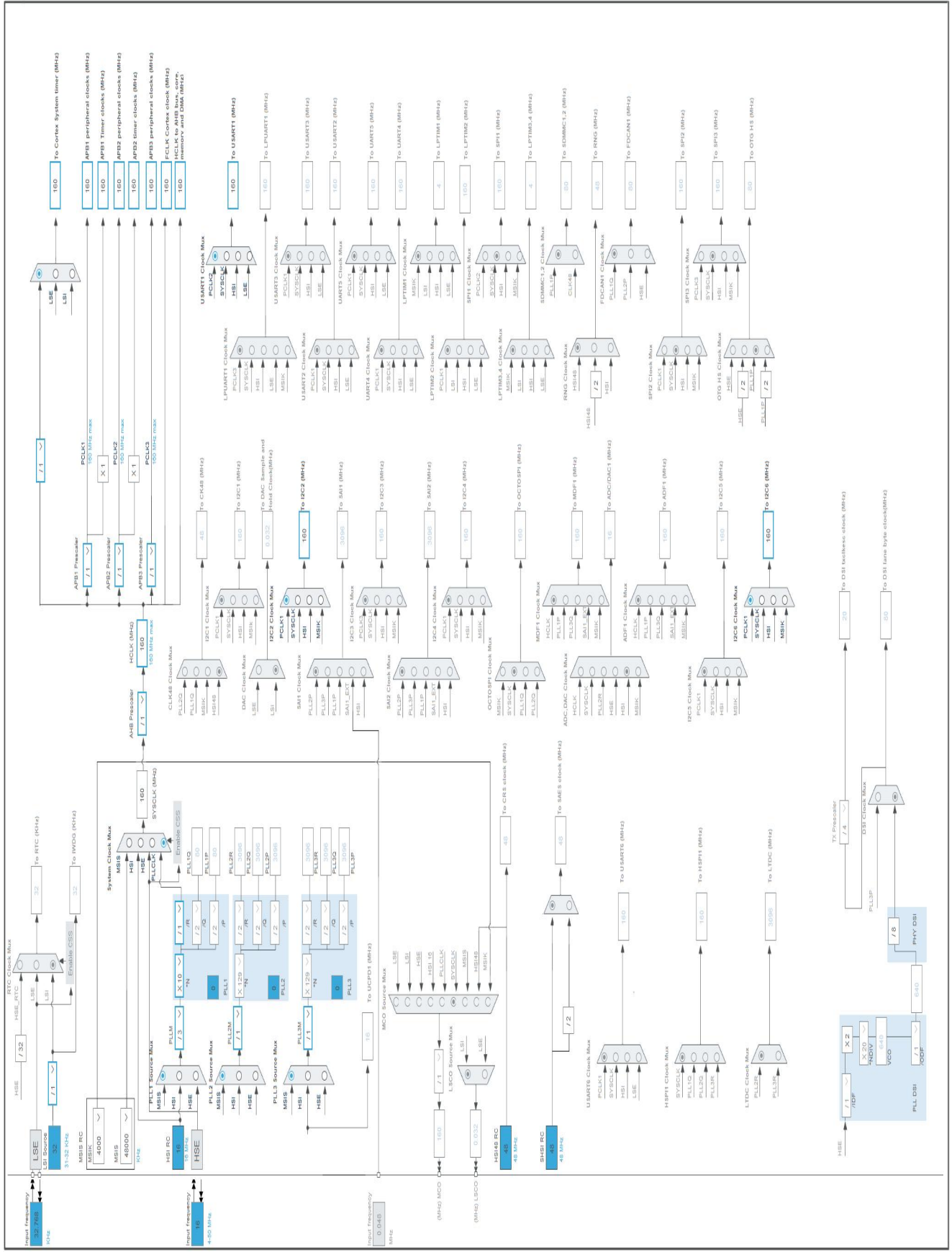
TFPGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A15	VSS	Power		
B1	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
C1	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
C2	VBAT	Power		
C9	PD1	I/O	I2C6_SCL	
D9	PD0	I/O	I2C6_SDA	
D12	PA10	I/O	USART1_RX	
E6	VDD11	Power		
E8	VDDIO2	Power		
E9	VDDUSB	Power		
E10	VSS	Power		
E11	VDD11	Power		
E12	PA9	I/O	USART1_TX	
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VDD	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD11USB	Power		
G5	VDDDSI	Power		
G6	VSSDSI	Power		
G10	VSS	Power		
G11	VDDIO2	Power		
H2	VSSDSI	Power		
H5	VDD11DSI	Power		
H6	VSSDSI	Power		
H10	VSS	Power		
H11	VDD	Power		
H15	VSS	Power		
J2	VSSDSI	Power		
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J15	VSS	Power		
K5	VREF-	Power		
K6	VSSA	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
L6	VDDA	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VSS	Power		
L11	VDD	Power		
M10	PB11	I/O	I2C2_SDA	
N1	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
N2	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
N12	PB10	I/O	I2C2_SCL	
P12	VSSMPS	Power		
R1	VSS	Power		
R2	NRST	Reset		
R11	VLXSMPS	Power		
R12	VDDSMPS	Power		
R13	VDD11	Power		
R15	VSS	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MOUNIA
Project Folder	C:\Users\talib\STM32CubeIDE\workspace_1.14.2\MOUNIA
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_U5 V1.5.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART1_UART_Init	USART1
4	MX_I2C2_Init	I2C2
5	MX_DCACHE1_Init	DCACHE1
6	MX_DCACHE2_Init	DCACHE2
7	MX_I2C6_Init	I2C6

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32U5
Line	STM32U599/5A9
MCU	STM32U5A9NJHxQ
Datasheet	not yet available

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

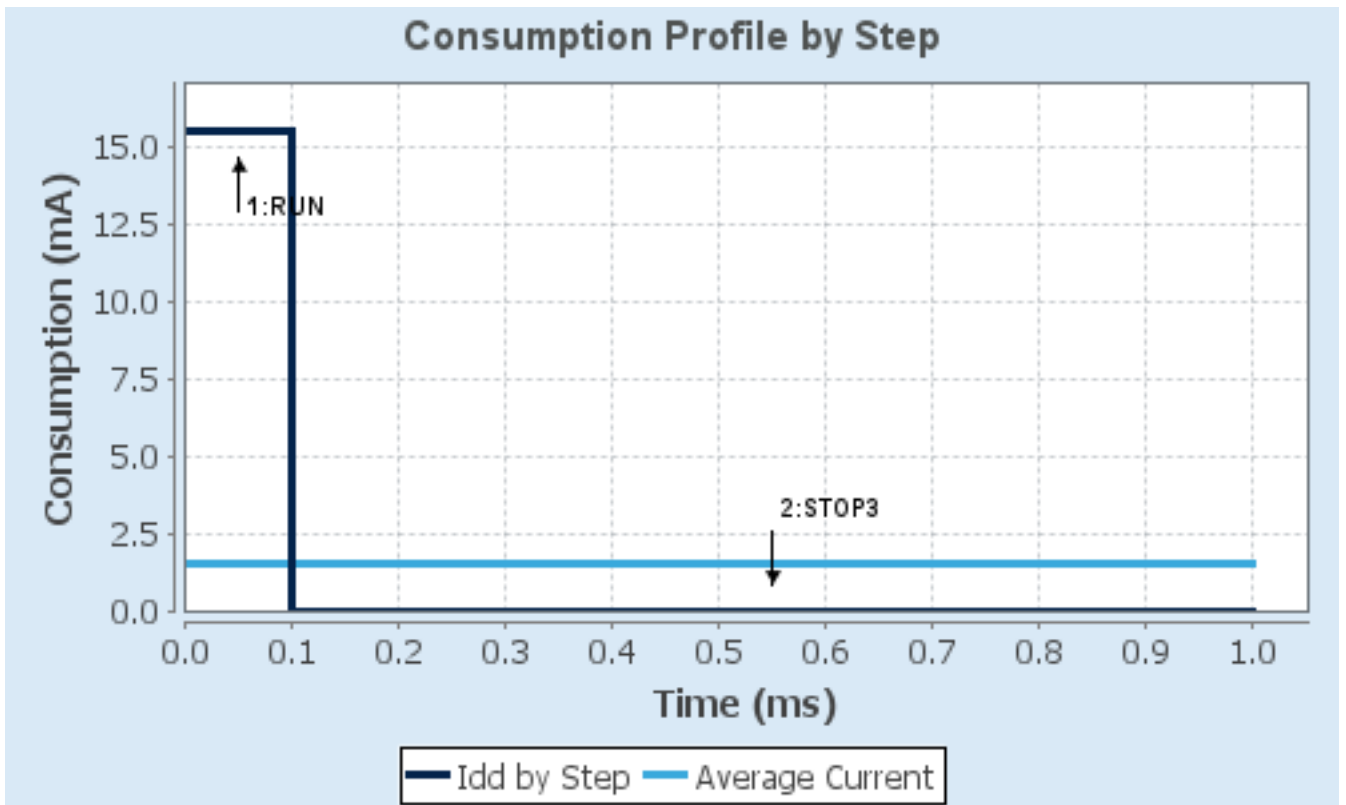
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP3
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Medium	NoRange/SMPS
Fetch Type	FLASH- PwrDwnBank2/ART/Cache- 2Ways/AlgoType- ReducedCode	FLASH
CPU Frequency	160 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL RAM RETENTION	ALL_CLOCKS_OFF
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	15.5 mA	1.85 μ A
Duration	0.1 ms	0.9 ms
DMIPS	240.0	0.0
Ta Max	138.74	140
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1.55 mA
Battery Life	2 months, 30 days, 5 hours	Average DMIPS	24.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. DCACHE1

mode: Activated

2.1.1. Parameter Settings:

Basic Parameters:

DCACHE Read Burst Type	DCACHE READ BURST WRAP
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2.2. DCACHE2

mode: Activated

2.2.1. Parameter Settings:

Basic Parameters:

DCACHE Read Burst Type	DCACHE READ BURST WRAP
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2.3. I2C2

I2C: I2C

2.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Disabled *
Timing	0x30909FEE *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

Autonomous Mode:

Autonomous Mode	Disable
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2.4. I2C6

I2C: I2C

2.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x30909DEC *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

Autonomous Mode:

Autonomous Mode	Disable
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2.5. LPBAM

mode: LPBAM Scenario uses resources from Smart Run Domain only

mode: LPBAM Scenario is hosted by LPDMA1

2.6. LPBAMQUEUE

mode: QUEUE MODE

2.6.1. Parameter Settings:

DMA Channel Configuration:

Priority	Low
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DMA Channel Interrupt Configuration:

Data Transfer Error Interrupt	Disable
Update Link Error Interrupt	Disable
User Setting Error Interrupt	Disable
Transfer Complete Interrupt	Disable

Timebase Source: SysTick

2.11. USART1

Mode: Asynchronous

2.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Autonomous Mode	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C2	PB11	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C6	PD1	I2C6_SCL	Alternate Function Open Drain	Pull-up *	Low	
	PD0	I2C6_SDA	Alternate Function Open Drain	Pull-up *	Low	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	

3.2. GPDMA1

3.3. LINKEDLIST

3.4. LPDMA1

3.5. NVIC configuration

3.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
Flash non-secure global interrupt		unused	
RCC non-secure global interrupt		unused	
I2C2 Event interrupt		unused	
I2C2 Error interrupt		unused	
USART1 global interrupt		unused	
FPU global interrupt		unused	
Data cache global interrupt		unused	
I2C6 Error interrupt		unused	
I2C6 Event interrupt		unused	
DCACHE2 Data cache global interrupt		unused	

3.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Utilities	Other
CORTEX_M33 ✓			I2C2 ✓					PWR ✓	LINKEDLIST	
DCACHE1 ✓			I2C6 ✓							
DCACHE2 ✓			USART1 ✓							
GPDMA1										
GPIO ✓										
LPDMA1										
NVIC ✓										
RCC ✓										
SYS ✓										

5. Docs & Resources

Type	Link
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