2250-channel 8-bit Source Driver and GIP Gate Driver for Color Amorphous TFT-LCDs

Specification
Preliminary

Table of Contents

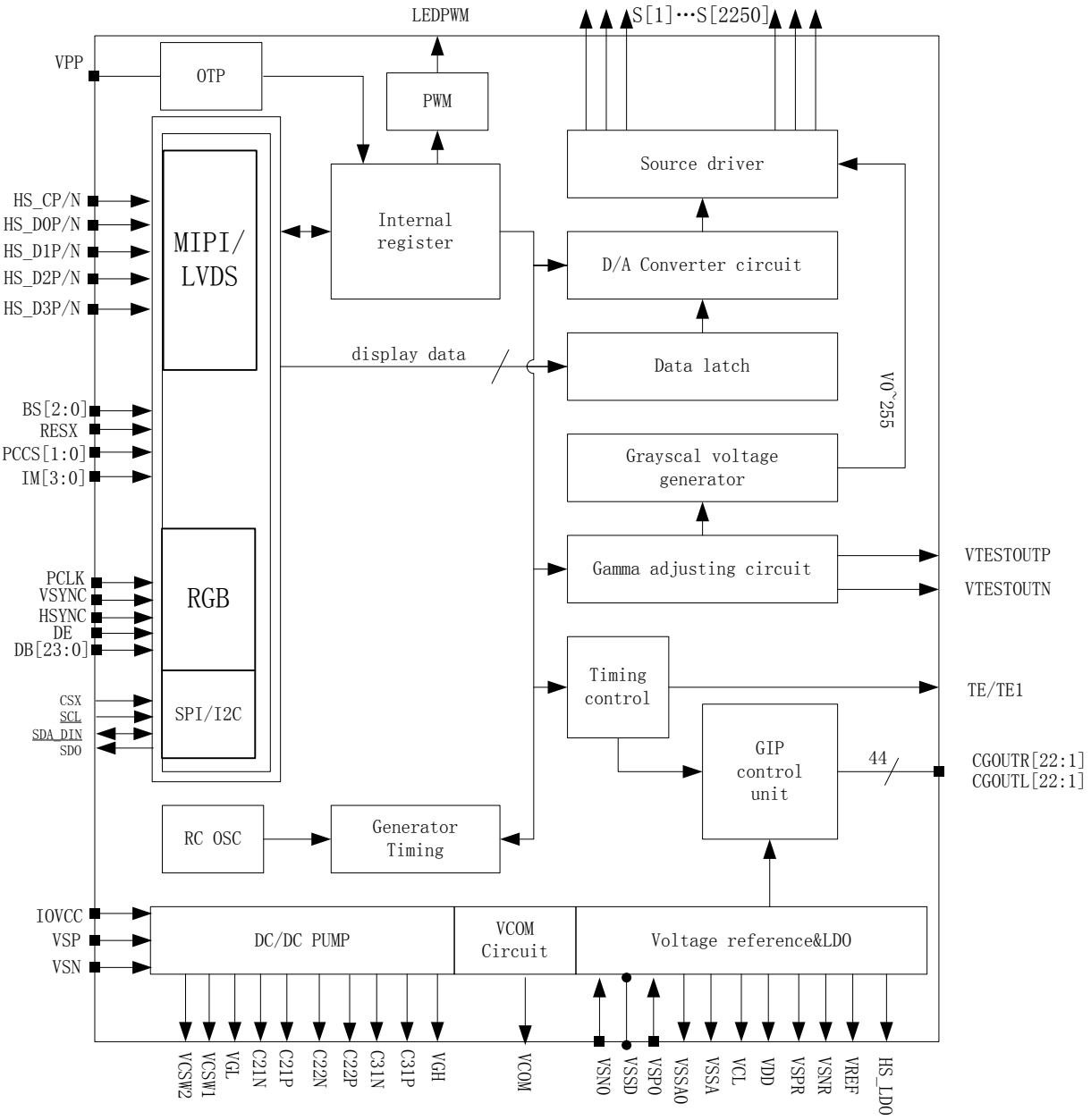
2 Features

- One-chip solution for color a-si TFT LCD
  Display Resolution
  - 750 x RGB x (1334, others), (Source output from S1 to S2250)
  - 720 x RGB x (1334, others), (Source output from S1 to S1080, S1171 to S2250)
  - 640 x RGB x (1334, others), (Source output from S1 to S960, S1291 to S2250)
  - (280+2x N) x RGB x (1334, others)

  (400 x RGB x 1280;640 x RGB x 1136;640 x RGB x 960;720 x RGB x 1280;750 x RGB x 1334)
- Display Data Memory: None (RAMless)
- System Interfaces
  - MIPI DSI (1/2/3/4 data lane): MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01). (1.5Gbps)
  - LVDS (4 data lane)
  - RGB(90MHz)
  - SPI(30Mbps)
  - I2C(500Kbps)
- Display Features
  - Outputs 256γ-corrected values and using an internal true 8-bit resolution D/A converter to achieve 16,777,216 colors
- On Chip Function
  - Support DC-VCOM driving scheme
  - RAMless driver with MIPI video mode
  - Built-in internal oscillator
  - Built–in OTP to store gamma, VCOM calibration and ID
  - Built–in OTP to store gamma, panel timing, and analog power setting
  - gamma output reference voltage level VSPR-VSSA: 2.5 ~ VSP -0.5V , VSNR-VSSA: -2.5 ~ VSN +0.5V
- Power Supply Range
  - I/O pads supply voltage (IOVCC): 1.65 ~ 3.3V
  - Positive source driver power (VSP): 4.5 ~ 6.5V
  - Negative source driver power (VSN): - 4.5 ~ - 6.5V

3 Block Diagram

3.1 Block Function



3.1.1 System interface

The Y13 supports the video data transmitted through the high-speed system interface, MIPI (Mobile Industry Processor Interface).

3.1.2 Grayscale voltage generating circuit

Y13 has true 8-bit resolution D/A converter, which generates 256 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by

4 Pin Description

4.1 Pin Definition

<table>
<tr><th colspan="3">Global Control Signal</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>RESX</td><td>I</td><td>Global Reset Signal. Active Low. If not used please connect it to IOVCC level</td></tr>
<tr><td>TE</td><td>O</td><td>Tear effect signal</td></tr>
<tr><td>TE1</td><td>O</td><td>Tear effect signal</td></tr>
<tr><td>IM[2：0]</td><td>I</td><td>
<table>
<tr><th>IM[2：0]</th><th>INTERFACE</th></tr>
<tr><td>3’b000</td><td>mipi</td></tr>
<tr><td>3’b001</td><td>spi + rgb</td></tr>
<tr><td>3’b010</td><td>i2c + rgb</td></tr>
<tr><td>3’b011</td><td>rgb</td></tr>
<tr><td>3’b100</td><td>spi + lvds</td></tr>
<tr><td>3’b101</td><td>i2c + lvds</td></tr>
<tr><td>3’b110</td><td>lvds</td></tr>
<tr><td>3’b111</td><td>reserved</td></tr>
</table>
</td></tr>
<tr><td>IM[3]</td><td>I</td><td>0 ，power on and display on generated based on user command ；1 ，power on and display on generated based on reset that don’t need user command</td></tr>
<tr><td>BS[2:0]</td><td>I</td><td>MIPI lane: D3P is the host sending end, HS_D0P is the of IC pa.
<table>
<tr><th>BS</th><th>3’b000</th><th>3’b001</th><th>3’b010</th><th>3’b011</th><th>3’b100</th><th>3’b101</th><th>3’b110</th><th>3’b111</th></tr>
<tr><td>HS_D0N</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>HS_D0P</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>HS_D1N</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td></tr>
<tr><td>HS_D1P</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>HS_CN</td><td>CN</td><td>CP</td><td>CN</td><td>CP</td><td>CN</td><td>CP</td><td>CN</td><td>CP</td></tr>
<tr><td>HS_CP</td><td>CP</td><td>CN</td><td>CP</td><td>CN</td><td>CP</td><td>CN</td><td>CP</td><td>CN</td></tr>
<tr><td>HS_D2N</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td></tr>
<tr><td>HS_D2P</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td></tr>
<tr><td>HS_D3N</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td></tr>
<tr><td>HS_D3P</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td></tr>
</table>
</td></tr>
<tr><td>PCCS[1:0]</td><td>I</td><td>Power mode:
<table>
<tr><th>PCCS[1:0]</th><th>IOVCC</th><th>VSP</th><th>VSN</th><th>VGH/VGL</th></tr>
<tr><td>2’b00</td><td>external input</td><td>external input</td><td>external input</td><td>external input</td></tr>
<tr><td>2’b01</td><td>external input</td><td>external input</td><td>external input</td><td>internal generate</td></tr>
<tr><td>2’b10</td><td>external input</td><td>external DC/DC</td><td>external DC/DC</td><td>internal generate</td></tr>
</table>
</td></tr>
</table>

		2'b11	external input	external input	external input	internal generate	
LEDPWM	O	Backlight lighting control pin, can connect to external LED driver IC.					
Panel driver Signals							
S[2250:1]	O	Output source driver signals. The D/A converted 256-gray-scale analog voltage output. Source output mapping with different resolution.					
CGOUT_L[22:1]	O	Gate control signals for panel in left side of IC					
CGOUT_R[22:1]	O	Gate control signals for panel in right side of IC					

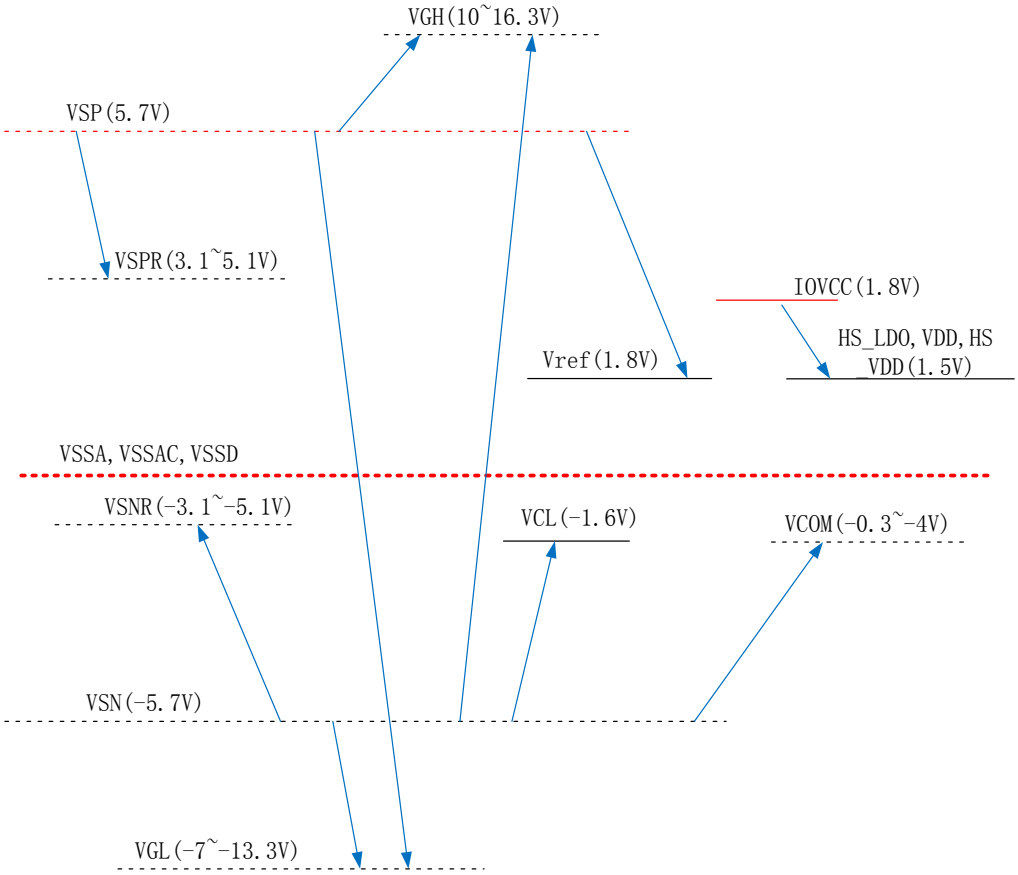
Power Supply and Regulator pins		
Pin Name	I/O	Descriptions
VCOM	O	VCOM signal output for panel
VSSA	G	Analog ground, connect to VSSD on FPC
VSSD	G	Digital ground
HS_LDO	O	1.5V LDO output for MIPI lower power circuit power supply, need connect a stabilizing capacitor to ground
IOVCC	I	1.8V power supply for digital interface
VDD	O	1.5V LDO output for digital power supply, need connect a stabilizing capacitor to ground
VCSW2	O	Connect to power IC
VCSW1	O	Connect to power IC
VPP	O	8.25V OTP high voltage power supply
VSP	I	5.7V voltage power supply Connect a stabilizing capacitor to ground
VSSA0	I	0V reference voltage, connect to VSSD on FPC
VSPR	O	4.8V LDO output for positive gamma reference, need connect a stabilizing capacitor to ground
VSNR	O	-4.8V LDO output for negative gamma reference, need connect a stabilizing capacitor to ground
VREF	O	1.8V output reference voltage, need connect a stabilizing capacitor to ground
VSN	I	-5.7V voltage power supply Connect a stabilizing capacitor to ground
VCL	O	-1.6V LDO negative output, need connect a stabilizing capacitor to ground
VSP0	I	5.7V reference voltage, connect to VSP on FPC
VSN0	I	-5.7V reference voltage, connect to VSN on FPC
VGH	O	15V power supply for GIP positive, connect astabilizing capacitor to ground
VGL	O	-10V power supply for GIP positive, connect a stabilizing capacitor to ground

C21P/C21N	-	Charge pump flying capacitor connection for VGH charge pump
C22P/C22N	-	Charge pump flying capacitor connection for VGL charge pump
C31P/C31N	-	Charge pump flying capacitor connection for VGL charge pump

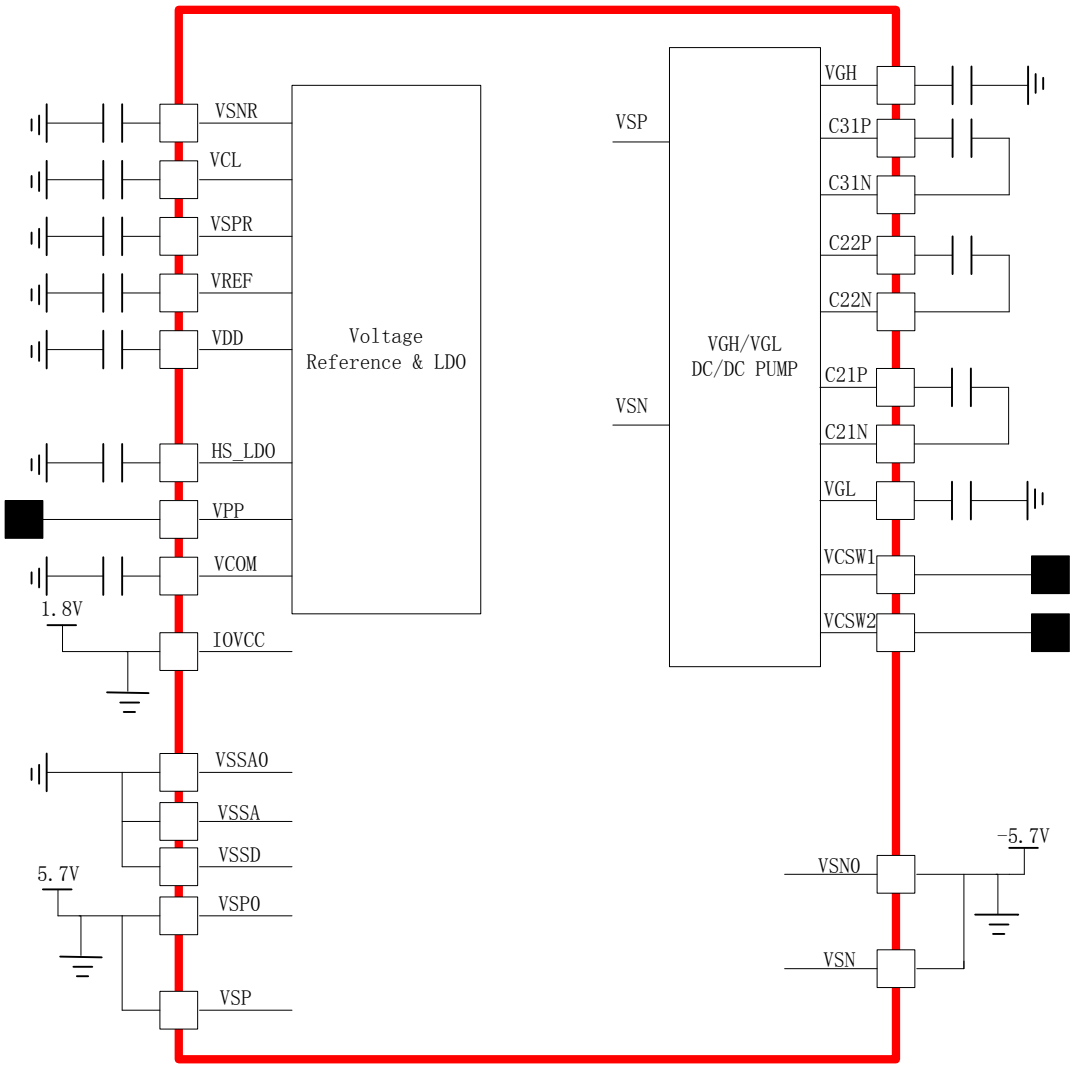
Test/Dummy Signal		
Pin Name	I/O	Descriptions
TESTA3/1/0	-	Test signal for debug, Please let them floating if not use
TS[11:0]	-	Test signal for debug, Please let them floating if not use
DUMMY	-	Dummy pins
DE_TC	-	Test signal for debug, Please let them floating if not use
OSC_IN	-	External clock for test.This pad is only used for cp test，and don't be packet in normal work mode
OSC_TE	-	Test signal for system clock select, This pad is only used for cp test， and don't be packet in normal work mode
VTESTOUTP	-	A test pin. This pin will output Gamma voltage. This pin can output on FPC
VTESTOUTN	-	A test pin. This pin will output Gamma voltage. This pin can output on FPC

4.2 Power Block Diagram

The following is the power supply generation scheme, Y13 consists of VSP（5.7V）and IOVCC（1.8V）as the input power supply, and others power supply levels are internal chip generate.


VGH(10~16.3V)
VSP(5.7V)
VSPR(3.1~5.1V)
IOVCC(1.8V)
HS_LDO, VDD, HS
VDD(1.5V)
Vref(1.8V)
VSSA, VSSAC, VSSD
VSNR(-3.1~-5.1V)
VCL(-1.6V)
VCOM(-0.3~-4V)
VSN(-5.7V)
VGL(-7~-13.3V)

4.3 Power Supply Peripheral Circuit



4.4 Power Supply Peripheral Component List

No.	Signal name	Values	Max ability	Note
1	VSN	4.7uF	10V	-
2	VDD	2.2uF	6.3V	TCON Power
3	VREF	1.0uF	6.3V	Regulator
4	VGH	1.0uF	25V	VGH Pump
5	C21P/C21N C22P/C22N	1.0uF	25V	
6	VGL	1.0uF	25V	VGL Pump
7	C31P/C31N	1.0uF	25V	

8	VCOM	2.2uF	10V	-
9	VCL	1.0uF	6.3V	-
10	VSPR	1.0uF	10V	-
11	VSNR	1.0uF	10V	-
12	HS_LDO	1.0uF	6.3V	-

5 Instructions

5.1 Outline

The Y13 supports high speed serial interface, MIPI, to configure the system via accessing command registers. While accessing the command registers, the information that indicates which register would be accessed should be sent first. After that, the new value can be updated via system interface. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.01.00 and D-PHY Version 1.00.00. Updating command instructions can also be accomplished by using all supporting system interfaces (MIPI, and I-80 8-bit parallel bus interface).

The Y13 has the following major categories of instructions:

(1). System function instructions (User Command Set).

(2). Customer Command List and Description (Manufacturer Command Set / Command 2).

Since updating these instructions are asynchronous to the internal clock of the Y13, the updating procedure will require no waiting cycles. Furthermore, the updating procedure will not interfere with the processing of the host controller, this makes instructions can be handled smoothly and efficiently.

The following contents of this chapter will describe the supported instructions in detail.

5.2 System Command List and Description

5.2.1 Introduction

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register will return to the default state. The commands 10h, 20h, 21h, 28h, 29h, 36h will be updated only during V-sync

while module is in the "Sleep Out" mode to avoid abnormal visual effects, and will be updated immediately in the "Sleep In" mode.

5.2.2 System Command List

Name	Hex	Write/Read/Commend	Function	Paramter umber	Transmission
NOP	00H	W	No Operation Command	0	LPDT/ HSDT
POFF	10H	W	Power Off Command	0	LPDT/ HSDT
PON	11H	W	Power On Command	0	LPDT/ HSDT
NSI	20H	W	No Src_Inv Command	0	LPDT/ HSDT
SI	21H	W	Src_Inv Command	0	LPDT/ HSDT
DOFF	28H	W	Display Off Command	0	LPDT/ HSDT
DON	29H	W	Display On Command	0	LPDT/ HSDT
DCTR	36H	W/R	Display Control Command	1	LPDT/ HSDT
BLWR	51H	W/R	Pwm Blacklight control	1	LPDT/ HSDT
BLRD	52H	R	Pwm Blacklight read	1	LPDT/ HSDT

Note: LPDT (Low Power Mode), HSDT (High Speed Mode)

5.2.3 NOP (00h) : No Operation Command

8'H00	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			nop command (00)with no parameter has no effect to display								

5.2.4 POFF (10H) : Power Off Command

8'H10	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			power off command(10) with no parameter is used to turn off power								

5.2.5 PON (11H): Power On Command

8'H11	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			power on command(11) with no parameter is used to turn on power								

5.2.6 NSI (20H): No Src_Inv Command

8'H20	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			no src_inv command(20) with no parameter is used to exit the invertion of black and white picture								

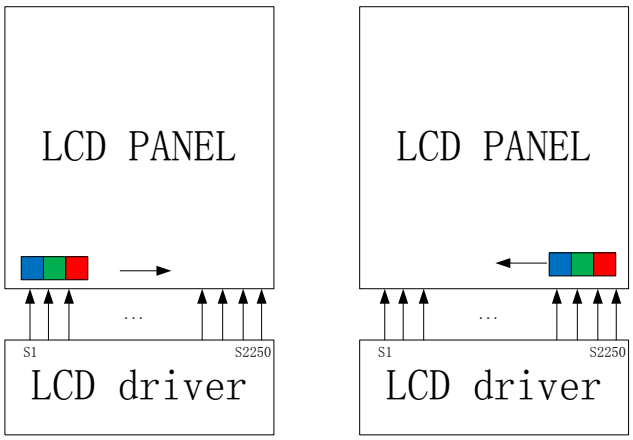
5.2.7 SI (21H): Src_Inv Command

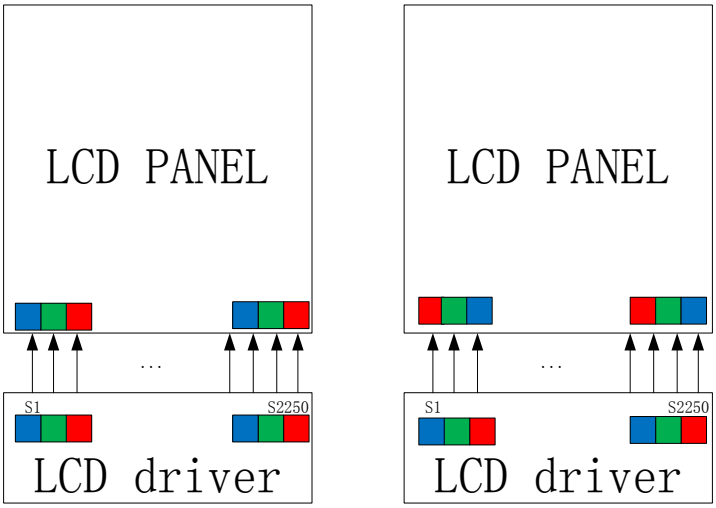
8'H21	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			src_inv command(21) with no parameter is used to enter the invertion of black and white picture								

5.2.8 DOFF (28H): Display Off Command

8'H28	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			display off command(28) with no parameter is used to turn off display								

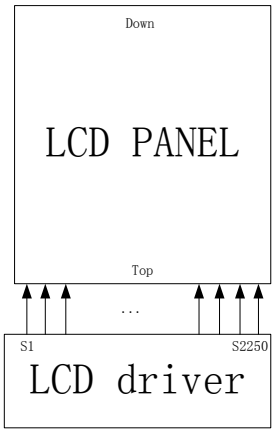
5.2.9 DCTR (36H): Display Control Command

8'H36	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑		cr_ca			cr_bgr			cr_gs	8'h00
description			**cr_ca**: order of data input shift 0:left to right 1:right to left  **cr_bgr**: order setting of RGB/BGR 0:RGB; 1:BGR								

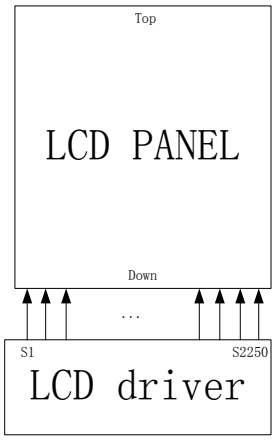


cr_gs: Flip vertical(Gate scan sequence);Select the Gate driver scan direction on panel module

0:top to down



1: down to top



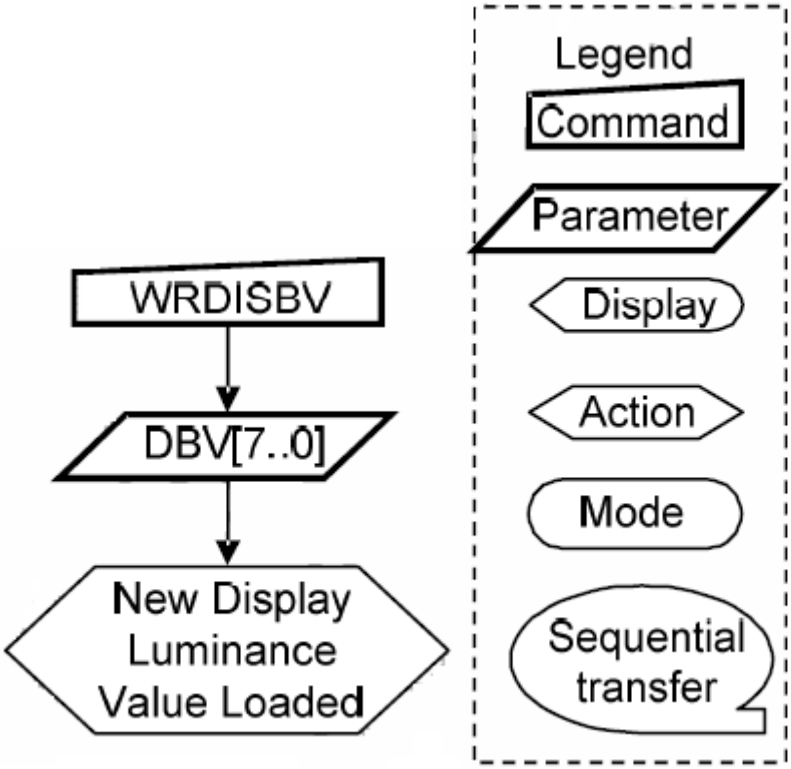
5.2.10 DON (29H): Display On Command

8'H29	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			display on command(29) with no parameter is used to turn on display								

5.2.11 WDB(51h)Write display brightness

8'H51	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	cr_bl [7:0]								00..FF
description			This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display modules pecification. In principle relationship is that 00h value means the lowest brightness and								

FFh value means the highest brightness.

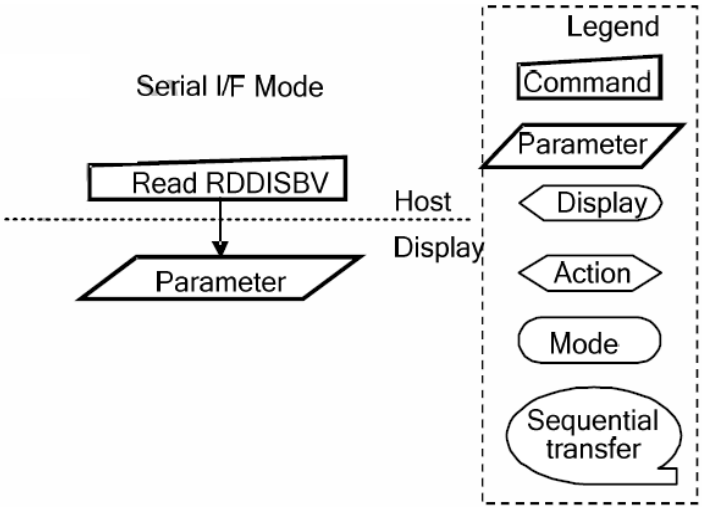


5.2.12 RDB(52h)Read display brightness value

8'H52	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	cr_bl[7:0]								XX

description

This command returns the brightness value of the display.
It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is.In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.



5.3 Customer Command List and Description (Manufacturer Command Set / Command 2)

5.3.1 Introduction

All manufacture command can be sent through mipi/I2C/SPI bus.

5.3.2 Customer Command List

Name	Hex	Write/ Read/ Commend	Function	Paramter Number	Transmission
SAOTS	A0H	C	Spi And Otp Test Setting (Not Otp Register)	12	Mipi/ SPI/I2C
DTS	A1H	C	Display Test Setting(Not Otp Register)	19	Mipi/ SPI/I2C
IACGUS	C1H	C	Interface And CGU Setting(Otp Register)	24	Mipi/ SPI/I2C
MRIDS	C2H	C	Mipi Read ID Setting(Otp Register)	22	Mipi/ SPI/I2C
IRGBS	C3H	C	Internal rgb Setting (Otp Register)	25	Mipi/ SPI/I2C
VCOMS	C4H	C	Vcom Setting(Otp Register)	2	Mipi/ SPI/I2C
AS1	DFH	C	Analog MIPI lane circuit Setting(Otp Register)	10	Mipi/ SPI/I2C
AS2	D0H	C	Analog other circuit Setting(Otp Register)	14	Mipi/ SPI/I2C
GS1	D1H	C	Gamma Setting1(Otp Register)	30	Mipi/ SPI/I2C
GS2	D2H	C	Gamma Setting2(Otp Register)	30	Mipi/ SPI/I2C
GS3	D3H	C	Gamma Setting3(Otp Register)	29	Mipi/ SPI/I2C
GS4	D4H	C	Gamma Setting4(Otp Register)	29	Mipi/ SPI/I2C
GIPS	D5H	C	GIP Setting(Otp Register)	26	Mipi/ SPI/I2C
GIPS2	D6H	C	GIP Setting2(Otp Register)	23	Mipi/ SPI/I2C
GIPSCANSET1	D7H	C	GIP left scan Setting for forward (Otp Register)	22	Mipi/ SPI/I2C
GIPSCANSET2	D8H	C	GIP right scan Setting for forward (Otp Register)	22	Mipi/ SPI/I2C
GIPSCANSET3	D9H	C	GIP left scan Setting for backward (Otp Register)	22	Mipi/ SPI/I2C
GIPSCANSET4	DDH	C	GIP right scan Setting for backward (Otp Register)	22	Mipi/ SPI/I2C
YUVSET	DEH	C	YUV exchange Setting(Otp Register)	20	Mipi/ SPI/I2C
OTPRD	F0H	R	OTP read at one byte mode (Not Otp Register)	1	Mipi/ SPI

OTPNUM	FEH	R	OTP read the byte number of used (Not Otp Register)	1	Mipi/ SPI

5.3.3 IACGUS (C1H) : Interface And CGU Setting(Otp Register)

8'HC1	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	cr_dsp_sel	cr_src_opt	cr_bgr_opt	cr_ret	cr_sync_sel	cr_err_en	cr_ln_sel		8'h12
par1	↑	↑	cr_tx_sel		cr_divi		cr_ecc_en	cr_term_sel			8'h80
par2	↑	↑	cr_ta_config[7:0]								8'h71
par3	↑	↑	cr_ta_config[15:8]								8'h05
par4	↑	↑	cr_pcdivh				cr_pcdivl				8'h44
par5	↑	↑	cr_sd_vfp								8'hb3
par6	↑	↑	cr_sd_vbp								8'h13
par7	↑	↑	cr_eq_width[9:8]		cr_sd_spa		cr_sd_chop_opt				8'h01
par8	↑	↑	-								8'h16
par9	↑	↑	cr_eq_sl								8'h20
par10	↑	↑	cr_sd_pol	cr_sd_op_en	-	-	-	-			8'h43
par11	↑	↑	-	-	-	-	cr_bl_clk_sel				8'h06
par12	↑	↑	-								8'h00
par13	↑	↑	cr_vgh_clk_sel1				-		-		8'h30
par14	↑	↑	cr_sd_bias_en	cr_dsh_shr	cr_ctrl_mod_sel		-		cr_ga_en	cr_dout_dig_en	8'hc0
par15	↑	↑	cr_sd_op_chop_opt	cr_inv_sel	cr_sa_clk_sel		cr_dsh_clk_dly				8'h80

par16	↑	↑	cr_vgh_clk_sel2		cr_dsh_reso[8:7]	8’h9a
par17	↑	↑	cr_dsh_reso[6:0]			8’h80
par18	↑	↑	-			8’h08
par19	↑	↑	-	cr_le_width		8’h0a
par20	↑	↑	-			8’h69
par21	↑	↑	-			8’h69
par22	↑	↑	--			8’h3f
par23	↑	↑			-	4’h0
Description			**cr_dsp_sel:** Display clock selection:1,pclk from output osc;0,pclk from internal generation. **cr_src_opt:** Black or white option: 0, inverse. **cr_bgr_opt:** RGB or BGR option: 0, BGR. **cr_ret:** Option register for return packet: 0,no return; 1, return. **cr_sync_sel:** The register option to select synchronous start. **cr_err_en**： the mipi low power return conflict error detect enable. **cr_ln_sel**： the mipi lane select. **cr_tx_sel:** lp_tx_clk selection. **cr_divi**: the division select of oscillator **cr_ecc_en**:enble of checking ecc **cr_term_sel:**The register option to select the hs_settle_d delay time that output to analog. **cr_ta_config:** The register to configure the turnaround every state time. **cr_pcdivh**: PCLKD high period **cr_pcdivl**: PCLKD low period**cr_sd_vbp:** the vertical back porch used for source timing. **cr_sd_vfp:** the vertical front porch used for source timing. **cr_sd_spa:** Decide the spacing from start pulse to sw signals . **cr_sd_chop_opt:** Select the line number to chop once. **cr_eq_sl:** Select start line for eq. cr_sd_pol:the enable to invert the source data polar,activity is 1 cr_sd_op_en:register for SD_OP_EN in test mode cr_bl_clk_sel：the clock frequence selection of bl_clk cr_vgh_clk_sel1：the selection of vgh charge pump clock frequence cr_sd_bias_en：register for output signal SD_BIAS_EN at test mode **cr_dsh_shr:** Read data sequential select: 1,reverse; 0, normal. cr_ctrl_mod_sel：select output power control clock signal cr_ga_en：register for output signal GA_EN at test mode **cr_sd_op_chop_opt:** An option ctrl for SD_OP_CHOP signal, if high output internal generate signal; if low output zero. **cr_inv_sel**: select the inversion mode. 00:frame inversion;			

	01:line inversion cr_sa_clk_sel：the selection of sample clock frequence cr_dsh_clk_dly：the selection of output dsh_clk signal delay cr_vgh_clk_sel2：the selection of vgh charge pump clock frequence **cr_lp_tx_sr:** low power tx SR adjust 00: 5pf loading, SR=344mv/ns 01: 20pf loading, SR=239mv/ns 10: 50pf loading, SR=169mv/ns 11: 70pf loading, SR=80mv/ns **cr_dsh_reso[8:0]:** Resolution selection,min:280,max:750 cr_le_width：the le pulse width adjust

5.3.4 MRIDS (C2H): Mipi Read ID Setting(Otp Register)

8'HC2	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	cr_id_entry								8'h87
par1	↑	↑	cr_id_dataid								8'h1a
par2	↑	↑	cr_id_par0								8'h0f
par3	↑	↑	cr_id_par1								8'h00
par4	↑	↑	cr_id_ecc								8'h16
par5	↑	↑	cr_id_pld0								8'ha1
par6	↑	↑	cr_id_pld1								8'hc3
par7	↑	↑	cr_id_pld2								8'hfe
par8	↑	↑	cr_id_pld3								8'h09
par9	↑	↑	cr_id_pld4								8'h06
par10	↑	↑	cr_id_pld5								8'h44
par11	↑	↑	cr_id_pld6								8'h09
par12	↑	↑	cr_id_pld7								8'h00
par13	↑	↑	cr_id_pld8								8'h00
par14	↑	↑	cr_id_pld9								8'h00
par15	↑	↑	cr_id_pld10								8'h00
par16	↑	↑	cr_id_pld11								8'h00
par17	↑	↑	cr_id_pld12								8'h00
par18	↑	↑	cr_id_pld13								8'h00
par19	↑	↑	cr_id_pld14								8'h00

par20	↑	↑	cr_id_pld15	8’h60
par21	↑	↑	cr_id_pld16	8’h6c
Description			these register is used to written data for mipi read id	

5.3.5 VS (C4H):Vcom Setting(Otp Register)

8’HC4	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	cr_vcom_adj[7:0]								8’h00
par1	↑	↑								cr_vcom_adj[8]	8’h01
Description			**cr_vcom_adj:** Worked with cr_vcom_offset to control vcom. VCOM= **cr_vcom_adj+/- cr_vcom_offset**[4:0]; **cr_vcom_offset**[5]=1 → subtract，**cr_vcom_offset**[5]=0 → add VCOM =**0x000H~0x1FDH** →VCOM=-0.3V-d*0.005； VCOM =**0x1FEH** →VCOM=VSSA； VCOM =**0x1FFH** →VCOM=hiz；							

5.3.6 AS1 (DFH):Analog MIPI lane circuit Setting (Otp Register)

8’HDF	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑		cr_ipost_adj				cr_ipre_adj			8’h44
par1	↑	↑		cr_vdd_adj				cr_tres_adj_c			8’h43
par2	↑	↑		cr_tres_adj_d1				cr_tres_adj_d0			8’h33
par3	↑	↑		cr_tres_adj_d3				cr_tres_adj_d2			8’h33

par4	↑	↑	cr_vih_adj			cr_vil_adj			6’h61
par5	↑	↑		cr_hsd_post_dly_d0		cr_hsd_pre_dly_d0			8’h48
par6	↑	↑		cr_hsd_post_dly_d1		cr_hsd_pre_dly_d1			8’h48
par7	↑	↑		cr_hsd_post_dly_d2		cr_hsd_pre_dly_d2			8’h48
par8	↑	↑		cr_hsd_post_dly_d3		cr_hsd_pre_dly_d3			8’h48
par9	↑	↑		cr_hs_lag_en_d	cr_hs_lag_adj_d		cr_hs_lag_en_c	cr_hs_lag_adj_c	8’h00
Description			**cr_ipost_adj:** Directly output to port MIPI_IPOST_ADJ , MIPI posterior amplifier current adjust 000: 25uA 001: 30uA 010: 35uA 011: 40uA 100: 45uA (default) 101: 50uA 110: 55uA 111: 60uA **cr_ipre_adj:** Directly output to port MIPI_IPRE_ADJ, MIPI previous amplifier current adjust 000: 10uA 001: 20uA 010: 30uA 011: 40uA 100: 50uA (default) 101: 60uA 110: 70uA 111: 80uA cr_vdd_adj **:VDD adjust register** **000:1.4v, 001: 1.45v, 010: 1.5v, 011: 1.55v,** **100: 1.6v, 101: 1.65v, 110: 1.7v, 111: 1.8v** **cr_tres_adj_d* :** Directly output to port MIPI_TRES_ADJ_D*. MIPI Data terminal matching resistance adjust 000: 80ohm 001: 90 ohm 010: 95 ohm 011: 100 ohm(default) 100: 105 ohm 101: 110 ohm 110: 115 ohm 111: 120 ohm **cr_vih_adj：** Directly output to port VIH_SEL. Adjust Low Power Receive mode detect input high voltage reference. VIH=725mV+ D*25mV **cr_vil_adj:** Directly output to port VIL_SEL. Adjust Low Power Receive mode detect input low voltage reference: VIL=525mV+D*25mV **cr_hsd_post_dly_d*:** Directly output to port HSD_POST_DLY_D*. High speed data posterior delay adjust. When HSD_PRE_DLY_ADJ<3:0> = 1111; TT corner ; Temperature: 27Deg Power : 1.5V								

	000: 395.9ps 001: 391.5ps 010: 387.7ps 011: 384.4ps 100: 381.6ps(default) 101: 379.1ps 110: 377ps 111: 375ps **cr_hsd_pre_dly_d*:** Directly output to port HSD_PRE_DLY_D*. High speed data previous delay adjust. When HSD_POS_DLY_ADJ<2:0> = 111; TT corner ; Temperature: 27Deg Power : 1.5V 0000: 428.5ps 0001: 420.9ps 0010: 414.4ps 0011: 408.8ps 0100: 404ps 0101: 400ps 0110: 396ps 0111: 392.4ps 1000: 389.6ps(default) 1001: 387ps 1010: 384.5ps 1011: 382.3ps 1100: 380.2ps 1101: 378.3ps 1110:376.6ps 1111: 375ps **cr_hs_lag_en_d:** Directly output to port HS_LAG_EN_D. High Speed hysteresis comparator lag enable register for data lane.0:disable(default) **cr_hs_lag_adj_d:** Directly output to port HS_LAG_ADJ_D. High Speed hysteresis comparator lag adjustment for data lane. **cr_hs_lag_en_c:** Directly output to port HS_LAG_EN_C. High Speed hysteresis comparator lag enable register for clock lane.0:disable(default) **cr_hs_lag_adj_c:** Directly output to port HS_LAG_ADJ_C. High Speed hysteresis comparator lag adjustment for clock lane.

5.3.7 AS2 (D0H):Analog other circuit Setting (Otp Register)

8'HD0	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default

par0	↑	↑	cr_iref_sel					cr_vpp_adj		8’h42
par1	↑	↑	cr_ldo_bias_reg	cr_vspr_en	cr_vspr_cap	cr_vsnr_en	cr_vsnr_cap		cr_vcl_en	8’h51
par2	↑	↑		cr_vcl_adj			cr_bgr_caps	cr_hs_ldo_adj		6’h24
par3	↑	↑	cr_vspr_adj[7:0]							8’h68
par4	↑	↑	cr_vsnr_adj[7:0]							8’h68
par5	↑	↑	cr_vspr_adj[8]	cr_sd_ib_adj			cr_vsnr_adj[8]	cr_sd_vb_adj		8’hcc
par6	↑	↑	cr_dly_d3_lvds		cr_dly_d2_lvds		cr_dly_d1_lvds		cr_dly_d0_lvds	8’h55
par7	↑	↑	cr_bgr_chop_sw	cr_vgh_adj						8’h32
par8	↑	↑	cr_cp_vgh_sw	cr_vgl_adj						8’h5e
par9	↑	↑	cr_vghl_sw	cr_iref_adj_lvds			cr_cp_vgl_sw	cr_pclk_phase_adj_pll		8’h40
par10	↑	↑	cr_phase_pll		cr_delay_pll			cr_ich_pll		8’hda
par11	↑	↑	cr_osc_trim				cr_sd_chop_adj			8’h83
par12	↑	↑		cr_vcd_adj				cr_vcm_sel		8’h17
par13	↑	↑		cr_gan_bias_adj				cr_gap_bias_adj		8’h33
Description			**cr_iref_sel:** Directly output to port IREF_SEL. Adjust High Speed Receiver current reference: I_{HS}=(3uA+D*1uA)*2 . **cr_vpp_adj:** adjust vpp voltage. Vpp=8+d*0.1 **cr_vcl_adj:** adjust vcl voltage. Vcl=-1.4-d*0.1 **cr_vspr_adj:** adjust vspr voltage. Vspr=3+d*0.005 **cr_vsnr_adj:** adjust vsnr voltage. Vspr=-3-d*0.005							

	cr_vgh_adj: adjust vgh voltage. Vgh=10+d*0.1 **cr_vgl_adj:** adjust vgh voltage. Vgl=-7-d*0.1 **cr_ldo_bias_reg:** Directly output to port LDO_BIAS_REG. This is VDD_LDO and HS_LDO current adjust register. 0: 2uA；1: 3uA **cr_vspr_en:** Directly output to port VSPR_EN. When it is set to 0, the circuit doesn't work. **cr_vspr_cap:** Directly output to VSPR_CAP. 0: VSPR outer connect cap compensation; 1: VSPR internal compensation. **cr_vsnr_en:** Directly output to port VSNR_EN. When it is set to 0, the circuit doesn't work. **cr_vsnr_cap:** Directly output to VSNR_CAP. 0: VSNR outer connect cap compensation; 1: VSNR internal compensation. **cr_vcl_en:** Directly output to port VCL_EN. When it is set to 0, the circuit doesn't work. **cr_bgr_caps:** Directly output to port BGR_CAPS. 0: Bandgap doesn't need compensation; 1: Bandgap internal compensation. **cr_hs_ldo_adj:** Directly output to port HS_LDO_ADJ. HS_LDO adjust register. 000: 1.4V 001: 1.45V 010: 1.5V 011: 1.55V 100: 1.6V 101: 1.65V 110: 1.7V 111: 1.8V **cr_sd_ib_adj:** Directly output to port SD_IB_ADJ. Source bias current adjust: current=(1+D)uA **cr_sd_vb_adj:** Directly output to port SD_VB_ADJ. Source bias voltage adjust.

current=1.062uA+D*0.0625uA

cr_bgr_chop_sw: Directly output to port BGR_CHOP_SW.

00: 356KHz 01: 712KHz 1x: no chop

cr_cp_vgh_sw: Directly output to port CP_VGH_SW. VGH charge pump value control signal.

00:VGH=VSPC-VSNC

01:VGH=2*VSPC-VSNC

10:VGH=2*VSPC-2*VSNC

11:VGH=3*VSPC-2*VSNC

cr_cp_vgl_sw: Directly output to port CP_VGL_SW. VGL charge pump value control signal.

0:VGL=VSNC-VSPC

1:VGL=2*VSNC-VSPC

cr_vghl_sw: Directly output to port VGHL_SW. Select which CP charge pump. 0, CP work; 1, CPI work.

cr_osc_trim: Directly output to port OSC_TRIM. 45MHz oscillator trimming register, default is 45MHz. (37+cr_osc_trim)M

cr_dly_d*_lvds: Directly output to port DLY_D*_LVDS. Adjust high speed lane's transmission delay. DELAY=0.14ns+0.07*D

cr_ich_pll: Directly output to ICH_PLL. PLL charge pump current adjustment,default is 10ua.

cr_phase_pll: Directly output to PHASE_PLL. The register is used to adjust the phase between pixel clock and high speed clock.

00: Phase 2; 01: Phase 3; 10: Phase 0; 11: Phase 1(default)

cr_delay_pll: Directly output to port DELAY_PLL. PLL high speed clock delay adjustment, default is 633ps.

000: 374ps; 001: 466ps; 010: 540ps; 011: 633ps;(default) 100: 767ps; 101: 860ps; 110: 933ps; 111: 1026ps

cr_pclk_phase_adj_pll: Directly output to port PCLK_PHASE_ADJ_PLL. PLL pixel clock phase delay adjustment.

	cr_gap_bias_adj: Directly output. Adjustment for positive polarity bias current. 000: 0.5uA 001: 1uA 010: 1.5uA 011: 2uA (default) 100: 2.5uA 101: 3uA 110:3.5uA 111:4uA **cr_gan_bias_adj:** Directly output.Adjustment for negative polarity bias current. 000: -0.5uA 001: -1uA 010: -1.5uA 011: -2uA (default) 100: -2.5uA 101: -3uA 110:-3.5uA 111:-4uA

5.3.8 GS1 (D1H): Gamma Setting1(Otp Register)

8'HD1	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	-			cr_vnh0_adj					8'h40
par1	↑	↑	-			cr_vnh1_adj					8'h00
par2	↑	↑	-			cr_vnh2_adj					8'h40
par3	↑	↑	cr_vnh3_adj								8'h00
par4	↑	↑	cr_vnh4_adj								8'he0
par5	↑	↑	cr_vnh5_adj								8'he0
par6	↑	↑	cr_vnh6_adj								8'h00
par7	↑	↑	cr_vnh7_adj								8'h00
par8	↑	↑	cr_vnl0_adj								8'h00
par9	↑	↑	cr_vnl1_adj								8'h00
par10	↑	↑	cr_vnl2_adj								8'h00
par11	↑	↑	cr_vnl3_adj								8'h00
par12	↑	↑	cr_vnl4_adj								8'h00
par13	↑	↑	cr_vnl5_adj								8'h00
par14	↑	↑	cr_vnl6_adj								8'h00
par15	↑	↑	cr_vnl7_adj								8'h00
par16	↑	↑	cr_vnm0_adj								8'h00
par17	↑	↑	cr_vnm1_adj								8'h00
par18	↑	↑	cr_vnm2_adj								8'h00
par19	↑	↑	cr_vnm3_adj								8'h00
par20	↑	↑	cr_vnm4_adj								8'h00
par21	↑	↑	cr_vnm5_adj								8'h00
par22	↑	↑	cr_vnm6_adj								8'h00
par23	↑	↑	cr_vnm7_adj								8'h00
par24	↑	↑	cr_vnm8_adj								8'h00

par25	↑	↑		cr_vnm9_adj	8’h00
par26	↑	↑		cr_vnm10_adj	8’h00
par27	↑	↑		cr_vnm11_adj	8’h00
par28	↑	↑		cr_vnm12_adj	8’h00
par29	↑	↑			4’h8
Description			**cr_vnh*_adj:** Directly output. Negative polarity gamma grayscale level adjustment. **cr_vnm*_adj:** Directly output. Negative polarity gamma grayscale level adjustment. **cr_vnl*_adj:** Directly output. Negative polarity gamma grayscale level adjustment.		

5.3.9 GS2 (D2H): Gamma Setting2(Otp Register)

8’HD2	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑				cr_vph0_adj					5’h00
par1	↑	↑				cr_vph1_adj					5’h00
par2	↑	↑				cr_vph2_adj					5’h00
par3	↑	↑				cr_vph3_adj					5’h00
par4	↑	↑				cr_vph4_adj					5’h00
par5	↑	↑				cr_vph5_adj					5’h00
par6	↑	↑				cr_vph6_adj					5’h00
par7	↑	↑				cr_vph7_adj					5’h00
par8	↑	↑				cr_vpl0_adj					5’h00
par9	↑	↑				cr_vpl1_adj					5’h00
par10	↑	↑				cr_vpl2_adj					5’h00
par11	↑	↑				cr_vpl3_adj					5’h00
par12	↑	↑				cr_vpl4_adj					5’h00
par13	↑	↑				cr_vpl5_adj					5’h00
par14	↑	↑				cr_vpl6_adj					5’h00

par15	↑	↑				cr_vpl7_adj					5'h00
par16	↑	↑				cr_vpm0_adj					5'h00
par17	↑	↑				cr_vpm1_adj					5'h00
par18	↑	↑				cr_vpm2_adj					5'h00
par19	↑	↑				cr_vpm3_adj					5'h00
par20	↑	↑				cr_vpm4_adj					5'h00
par21	↑	↑				cr_vpm5_adj					5'h00
par22	↑	↑				cr_vpm6_adj					5'h00
par23	↑	↑				cr_vpm7_adj					5'h00
par24	↑	↑				cr_vpm8_adj					5'h00
par25	↑	↑				cr_vpm9_adj					5'h00
par26	↑	↑				cr_vpm10_adj					5'h00
par27	↑	↑				cr_vpm11_adj					5'h00
par28	↑	↑				cr_vpm12_adj					5'h00
par29	↑	↑			cr_vcom_offset						6'h00
Description			**cr_vph*_adj:** Directly output. Positive polarity gamma grayscale level adjustment. **cr_vpm*_adj:** Directly output. Positive polarity gamma grayscale level adjustment. **cr_vpl*_adj:** Directly output. Positive polarity gamma grayscale level adjustment.								

5.3.10 GS3 (D3H): Gamma Setting3(Otp Register)

8'HD3	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑		cr_vph0							7'h00
par1	↑	↑		cr_vph1							7'h01
par2	↑	↑		cr_vph2							7'h10
par3	↑	↑		cr_vph3							7'h14
par4	↑	↑		cr_vph4							7'h16
par5	↑	↑		cr_vph5							7'h1b
par6	↑	↑		cr_vph6							7'h23

5.3.12 GIPS1 (D5H): GIP Setting1(Otp Register)

8'HD5	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	-								8'hFF
par1	↑	↑	-								8'h00
par2	↑	↑	-				cr_fix3	cr_fix2	cr_fix1	cr_fix0	8'haa
par3	↑	↑	-								8'hff
par4	↑	↑				cr_vst_pst1					8'h0d
par5	↑	↑				cr_vst_pst2					8'h2e
par6	↑	↑				cr_vst_pst3					8'h4f
par7	↑	↑				cr_vst_pst4					8'h70
par8	↑	↑				cr_vst_pst5					8'h85
par9	↑	↑				cr_vst_pst6					8'ha6
par10	↑	↑				cr_vst_pst7					8'hc7
par11	↑	↑				cr_vst_pst8					8'he8
par12	↑	↑									8'h1f
par13	↑	↑									8'h1f
par14	↑	↑									8'h1f
par15	↑	↑									8'h1f
par16	↑	↑									8'h1f
par17	↑	↑									8'h1f
par18	↑	↑									8'h1f
par19	↑	↑									8'h1f
par20	↑	↑		cr_hig_wdt				cr_low_wdt			8'h44
par21	↑	↑	-			-					5'h00
par22	↑	↑					-		-		4'h3
par23	↑	↑		cr_vst_wdt				cr_nl[10:8]			8'h45
par24	↑	↑	cr_nl[7:0]								8'h36
par25	↑	↑	-								8'h00
Description			**cr_fix*:** fw_l/r and bw_l/r setting. **cr_vst_pst1~8:** Delay to vst1~8 active. **cr_hig_sdt:** High period of ck/ckb.								

	cr_low_wdt: Low period of ck/ckb. **cr_vst_wdt:** High period of vst1/2/3/4/5/6/7/8. **cr_nl:** Number of display clock for one line.

5.3.13 GIPS2 (D6H): GIP Setting2 (Otp Register)

8'HD6	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑			cr_bp						6'h0d
par1	↑	↑				-					8'h14
par2						-					5'h14
par3	↑	↑	cr_gspf								8'h20
par4	↑	↑	cr_gsps								8'h20
par5	↑	↑	cr_gto								8'h83
par6	↑	↑					-				4'hf
par7	↑	↑	cr_rst_endr[7:0]								8'h0c
par8	↑	↑		cr_rst_endr[10:8]				cr_rst_endl[10:8]			8'h00
par9	↑	↑	cr_rst_endl[7:0]								8'h0c
par10	↑	↑	cr_rst_star[7:0]								8'h08
par11	↑	↑		cr_rst_star[10:8]				cr_rst_stal[10:8]			8'h00
par12	↑	↑	cr_rst_stal[7:0]								8'h08
par13	↑	↑		-				-			8'h23
par14	↑	↑		-				-			8'h45
par15	↑	↑		-				-			8'h67
par16	↑	↑		-				-			8'h01
par17	↑	↑	cr_vg_dly_r								8'h20
par18	↑	↑	cr_vg_dly_f								8'h20
par19	↑	↑				-					5'h0d
par20	↑	↑				-					5'h0e
par21	↑	↑				-					5'h05
par22	↑	↑				-					5'h06

Description	**cr_gspf:** the gip_vst signal posedge location at one line **cr_gsps:** the gip_vst signal negedge location at one line **cr_vg_dly_f:** the gip_clk signal posedge location at one line **cr_vg_dly_r:** the gip_clk signal negedge location at one line **cr_gto:** Frame cycle. **cr_bp:** Back porch of vsync. **cr_rst_star:** Delay to posedge of reset_r. **cr_rst_endr:** Delay to negedge of reset_r. **cr_rst_stal:** Delay to posedge of reset_l. **cr_rst_endl:** Delay to negedge of reset_l.

5.3.14 GIPS3 (D7H): GIP Setting3 (Otp Register)

8'HD7	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	cr_cgout_l_0_sel_f								5'h1f
par1	↑	↑	cr_cgout_l_1_sel_f								5'h1f
par2	↑	↑	cr_cgout_l_2_sel_f								5'h1f
par3	↑	↑	cr_cgout_l_3_sel_f								5'h1f
par4	↑	↑	cr_cgout_l_4_sel_f								5'h1f
par5	↑	↑	cr_cgout_l_5_sel_f								5'h1f
par6	↑	↑	cr_cgout_l_6_sel_f								5'h1f
par7	↑	↑	cr_cgout_l_7_sel_f								5'h1f
par8	↑	↑	cr_cgout_l_8_sel_f								5'h1f
par9	↑	↑	cr_cgout_l_9_sel_f								5'h1f
par10	↑	↑	cr_cgout_l_10_sel_f								5'h1f
par11	↑	↑	cr_cgout_l_11_sel_f								5'h1f
par12	↑	↑	cr_cgout_l_12_sel_f								5'h1f
par13	↑	↑	cr_cgout_l_13_sel_f								5'h1f
par14	↑	↑	cr_cgout_l_14_sel_f								5'h1f
par15	↑	↑	cr_cgout_l_15_sel_f								5'h1f
par16	↑	↑	cr_cgout_l_16_sel_f								5'h1f
par17	↑	↑	cr_cgout_l_17_sel_f								5'h1f
par18	↑	↑	cr_cgout_l_18_sel_f								5'h1f

par19	↑	↑		cr_cgout_l_19_sel_f	5'h1f
par20	↑	↑		cr_cgout_l_20_sel_f	5'h1f
par21	↑	↑		cr_cgout_l_21_sel_f	5'h1f

description

cr_cgout_l_0_sel_f：in the positive sweep mode, select the signal output from the left 1 gip pad.

cr_cgout_l_1_sel_f：in the positive sweep mode, select the signal output from the left 2 gip pad.

……

cr_cgout_l_21_sel_f：in the positive sweep mode, select the signal output from the left 22 gip pad.

The signal selection list is as follows:

Register value	Output signal
0	VST0
1	VST1
2	VST2
3	VST3
4	VST4
5	VST5
6	VST6
7	VST7
8	CLK0
9	CLK1
10	CLK2
11	CLK3
12	CLK4
13	CLK5
14	CLK6
15	CLK7
16	GPWR1
17	GPWR2
18	GPWR3
19	GPWR4
20	TPE1

	21	TPE2
	22	RST_L
	23	RST_R
	24	FW_L
	25	FW_R
	26	BW_L
	27	BW_R
	28	1’b1
	29	1’b0
	30	1’b0
	31	1’b0

5.3.15 GIPS 4(D8H): GIP Setting4 (Otp Register)

8’HD8	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑				cr_cgout_r_0_sel_f					5’h1f
par1	↑	↑				cr_cgout_r_1_sel_f					5’h1f
par2	↑	↑				cr_cgout_r_2_sel_f					5’h1f
par3	↑	↑				cr_cgout_r_3_sel_f					5’h1f
par4	↑	↑				cr_cgout_r_4_sel_f					5’h1f
par5	↑	↑				cr_cgout_r_5_sel_f					5’h1f
par6	↑	↑				cr_cgout_r_6_sel_f					5’h1f
par7	↑	↑				cr_cgout_r_7_sel_f					5’h1f
par8	↑	↑				cr_cgout_r_8_sel_f					5’h1f
par9	↑	↑				cr_cgout_r_9_sel_f					5’h1f
par10	↑	↑				cr_cgout_r_10_sel_f					5’h1f
par11	↑	↑				cr_cgout_r_11_sel_f					5’h1f
par12	↑	↑				cr_cgout_r_12_sel_f					5’h1f
par13	↑	↑				cr_cgout_r_13_sel_f					5’h1f
par14	↑	↑				cr_cgout_r_14_sel_f					5’h1f
par15	↑	↑				cr_cgout_r_15_sel_f					5’h1f
par16	↑	↑				cr_cgout_r_16_sel_f					5’h1f

par17	↑	↑		cr_cgout_r_17_sel_f	5'h1f
par18	↑	↑		cr_cgout_r_18_sel_f	5'h1f
par19	↑	↑		cr_cgout_r_19_sel_f	5'h1f
par20	↑	↑		cr_cgout_r_20_sel_f	5'h1f
par21	↑	↑		cr_cgout_r_21_sel_f	5'h1f
description	cr_cgout_r_0_sel_f：in the positive sweep mode, select the signal output from the right 1 gip pad. cr_cgout_r_1_sel_f：in the positive sweep mode, select the signal output from the right 2 gip pad. …… cr_cgout_r_21_sel_f：in the positive sweep mode, select the signal output from the right 22 gip pad. The signal selection list is the same as the command D7.				

5.3.16 GIPS5 (D9H): GIP Setting5 (Otp Register)

8'HD9	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	cr_cgout_l_0_sel_b								5'h1f
par1	↑	↑	cr_cgout_l_1_sel_b								5'h1f
par2	↑	↑	cr_cgout_l_2_sel_b								5'h1f
par3	↑	↑	cr_cgout_l_3_sel_b								5'h1f
par4	↑	↑	cr_cgout_l_4_sel_b								5'h1f
par5	↑	↑	cr_cgout_l_5_sel_b								5'h1f
par6	↑	↑	cr_cgout_l_6_sel_b								5'h1f
par7	↑	↑	cr_cgout_l_7_sel_b								5'h1f
par8	↑	↑	cr_cgout_l_8_sel_b								5'h1f
par9	↑	↑	cr_cgout_l_9_sel_b								5'h1f
par10	↑	↑	cr_cgout_l_10_sel_b								5'h1f
par11	↑	↑	cr_cgout_l_11_sel_b								5'h1f
par12	↑	↑	cr_cgout_l_12_sel_b								5'h1f
par13	↑	↑	cr_cgout_l_13_sel_b								5'h1f
par14	↑	↑	cr_cgout_l_14_sel_b								5'h1f
par15	↑	↑	cr_cgout_l_15_sel_b								5'h1f
par16	↑	↑	cr_cgout_l_16_sel_b								5'h1f

par17	↑	↑		cr_cgout_l_17_sel_b	5'h1f
par18	↑	↑		cr_cgout_l_18_sel_b	5'h1f
par19	↑	↑		cr_cgout_l_19_sel_b	5'h1f
par20	↑	↑		cr_cgout_l_20_sel_b	5'h1f
par21	↑	↑		cr_cgout_l_21_sel_b	5'h1f
description	cr_cgout_l_0_sel_b：in the anti-sweep mode, select the signal output from the left 1 gip pad. cr_cgout_l_1_sel_b：in the anti-sweep mode, select the signal output from the left 2 gip pad. …… cr_cgout_l_21_sel_b：in the anti-sweep mode, select the signal output from the left 22 gip pad. The signal selection list is the same as the command D7.				

5.3.17 GIPS6 (DDH): GIP Setting6 (Otp Register)

8'HDD	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑				cr_cgout_r_0_sel_b					5'h1f
par1	↑	↑				cr_cgout_r_1_sel_b					5'h1f
par2	↑	↑				cr_cgout_r_2_sel_b					5'h1f
par3	↑	↑				cr_cgout_r_3_sel_b					5'h1f
par4	↑	↑				cr_cgout_r_4_sel_b					5'h1f
par5	↑	↑				cr_cgout_r_5_sel_b					5'h1f
par6	↑	↑				cr_cgout_r_6_sel_b					5'h1f
par7	↑	↑				cr_cgout_r_7_sel_b					5'h1f
par8	↑	↑				cr_cgout_r_8_sel_b					5'h1f
par9	↑	↑				cr_cgout_r_9_sel_b					5'h1f
par10	↑	↑				cr_cgout_r_10_sel_b					5'h1f
par11	↑	↑				cr_cgout_r_11_sel_b					5'h1f
par12	↑	↑				cr_cgout_r_12_sel_b					5'h1f
par13	↑	↑				cr_cgout_r_13_sel_b					5'h1f
par14	↑	↑				cr_cgout_r_14_sel_b					5'h1f
par15	↑	↑				cr_cgout_r_15_sel_b					5'h1f

par16	↑	↑		cr_cgout_r_16_sel_b	5'h1f
par17	↑	↑		cr_cgout_r_17_sel_b	5'h1f
par18	↑	↑		cr_cgout_r_18_sel_b	5'h1f
par19	↑	↑		cr_cgout_r_19_sel_b	5'h1f
par20	↑	↑		cr_cgout_r_20_sel_b	5'h1f
par21	↑	↑		cr_cgout_r_21_sel_b	5'h1f
description			cr_cgout_r_0_sel_b：in the anti-sweep mode, select the signal output from the left 1 gip pad. cr_cgout_r_1_sel_b：in the anti-sweep mode, select the signal output from the left 2 gip pad. …… cr_cgout_r_21_sel_b： in the anti-sweep mode, select the signal output from the left 22 gip pad. The signal selection list is the same as the command D7.		

6 Functions

6.1 MIPI-DSI Interface

6.1.1 General description

The communication can be separated into two different levels between the host and the display module:

– Interface Level : Low level communication

– Packet level : High level communication

6.1.2 Interface level communication

6.1.2.1 General

The display module uses data and clock lane differential pairs for DSI . Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode. Data lane1/2/3 can be driven High Speed mode only.

-	Lane support mode	MPU(Host) OTM0000A(Slave)

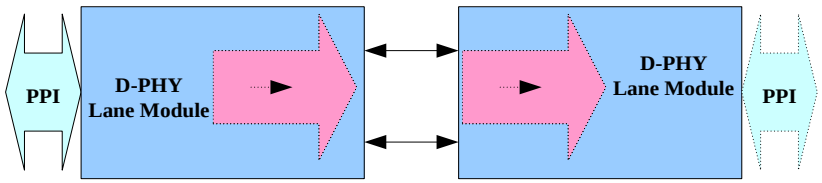
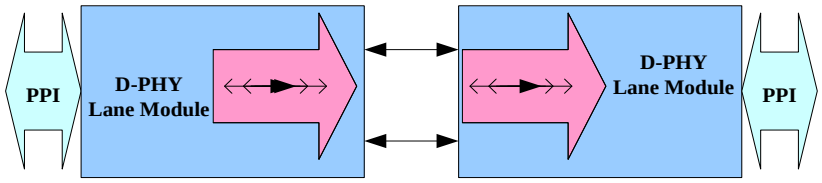
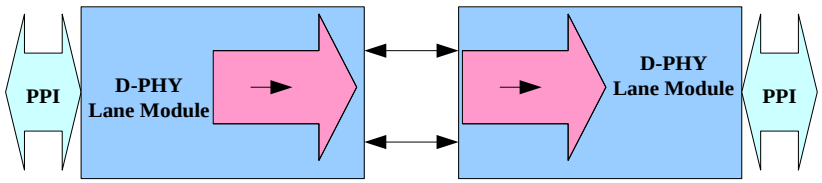
Clock Lane	Unidirectional lane • High-Speed Clock only •SimplifiedEscape Mode (ULPS Only)	
Data Lane0	Bi-directional lane • Forward high-speed only •Bi-directional Escape Mode • Bi-direction LPDT	
Data Lane1/ 2/3	Unidirectional lane • Forward high-speed only • Simplified Escape Mode (ULPS Only)	

Table: Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

6.1.2.2 DSI-CLK lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11),

Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

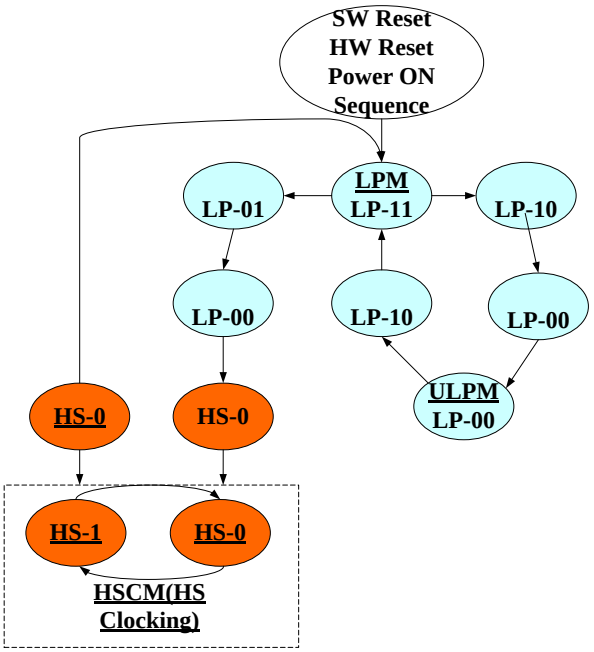


Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

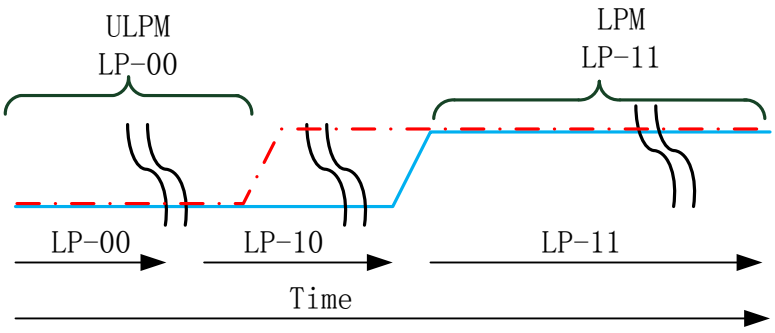


Figure:From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

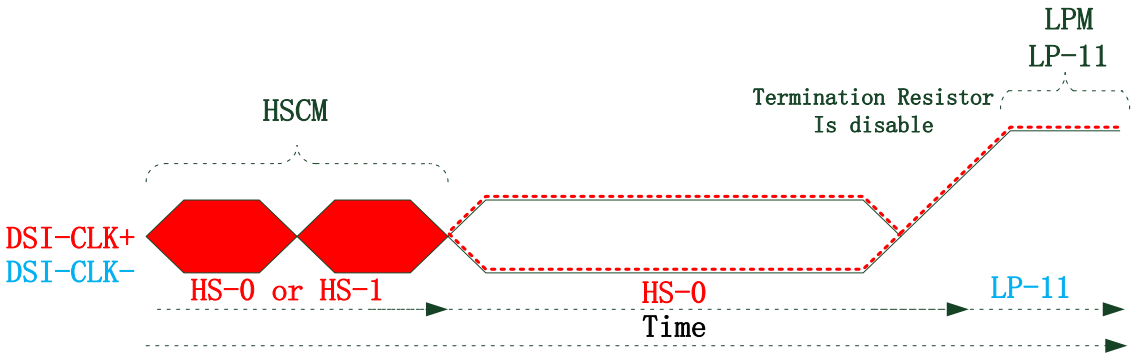


Figure: From HSCM to LPM

All three mode changes are illustrated a flow chart below.

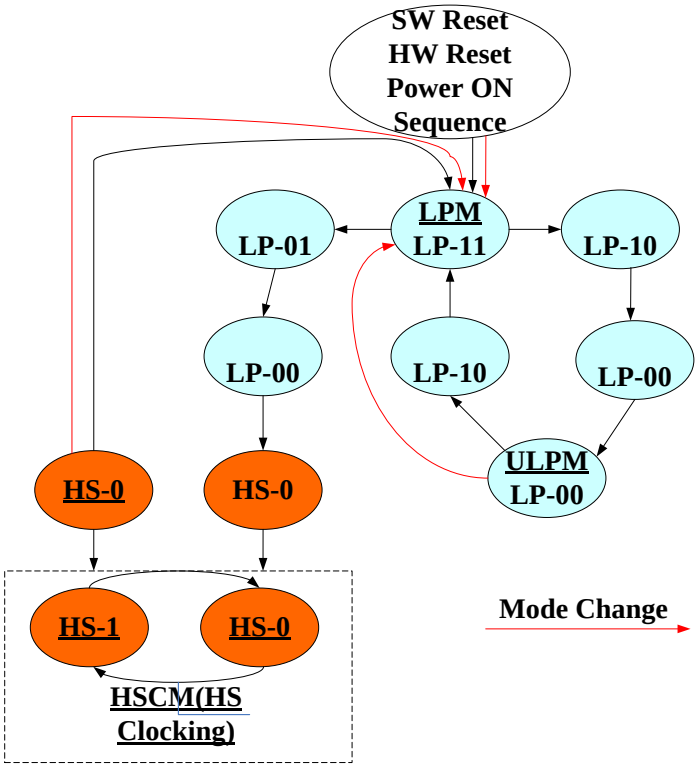


Figure: All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

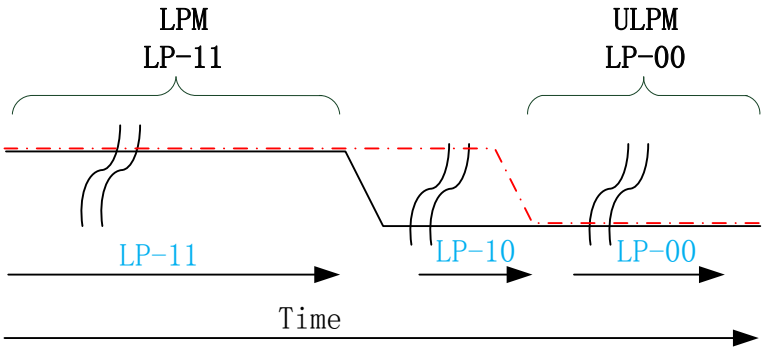


Figure: From LPM to UPLM

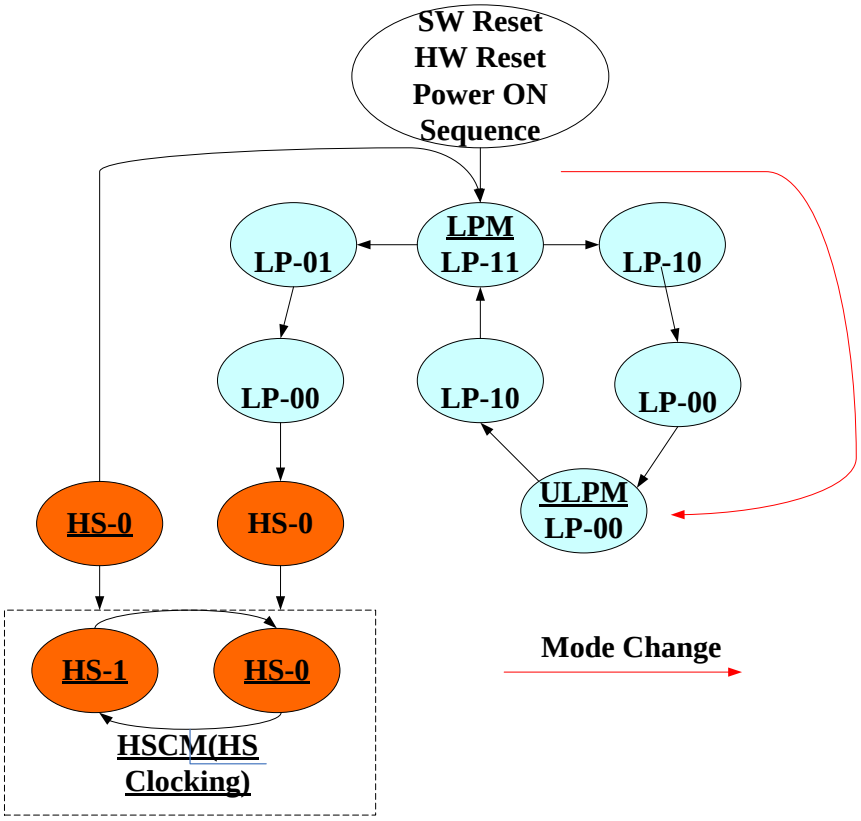


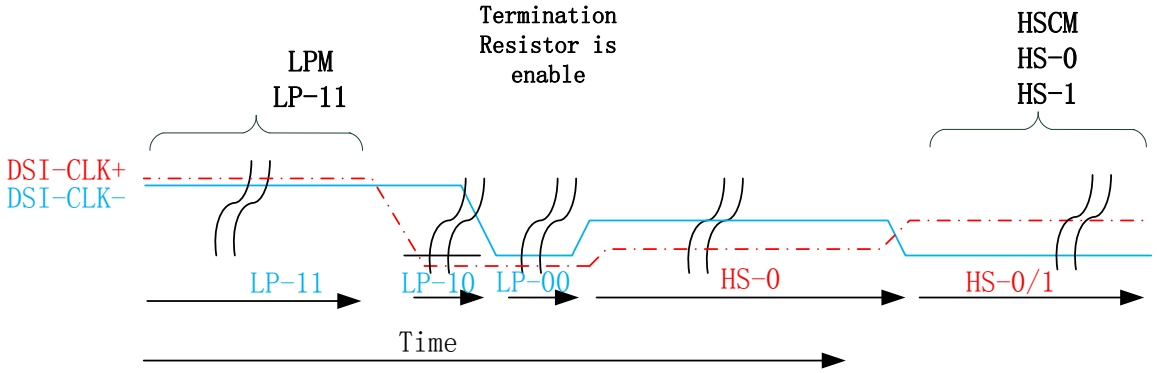
Figure:The mode change from LPM to UPLM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01

=>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.



Figur

e: From LPM to HSCM

The mode change is also illustrated below:

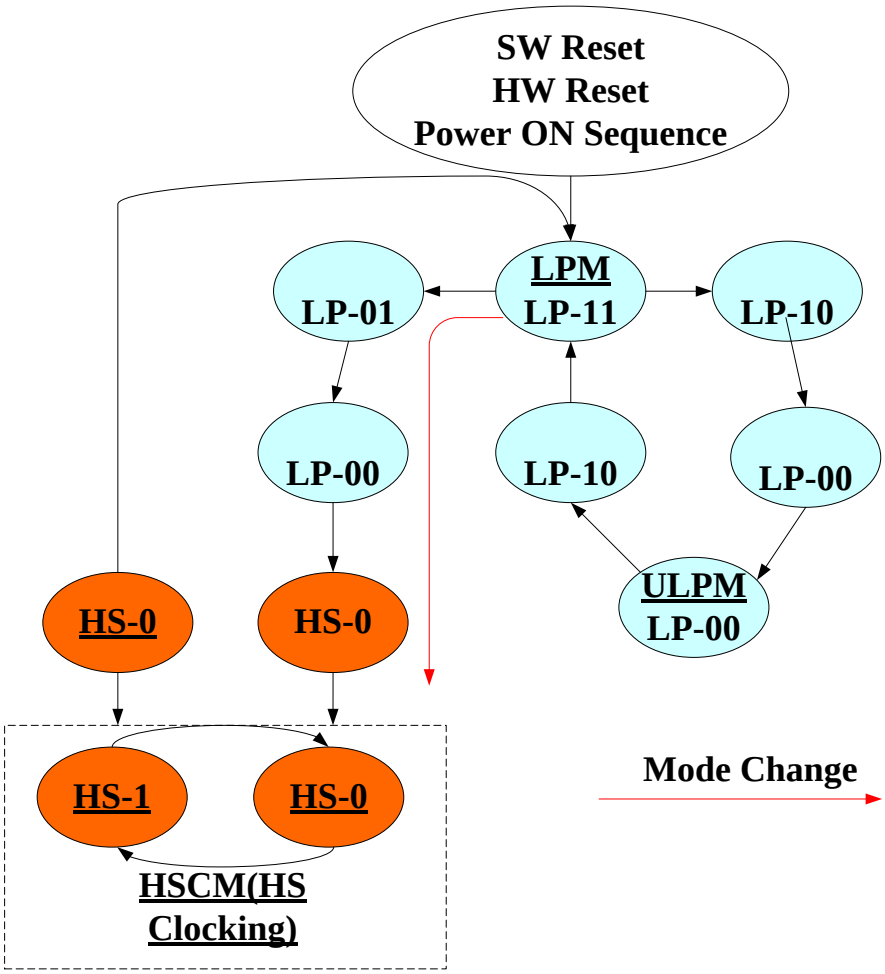


Figure:Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

– Even number of transitions
– Start state is HS-0
– End state is HS-0

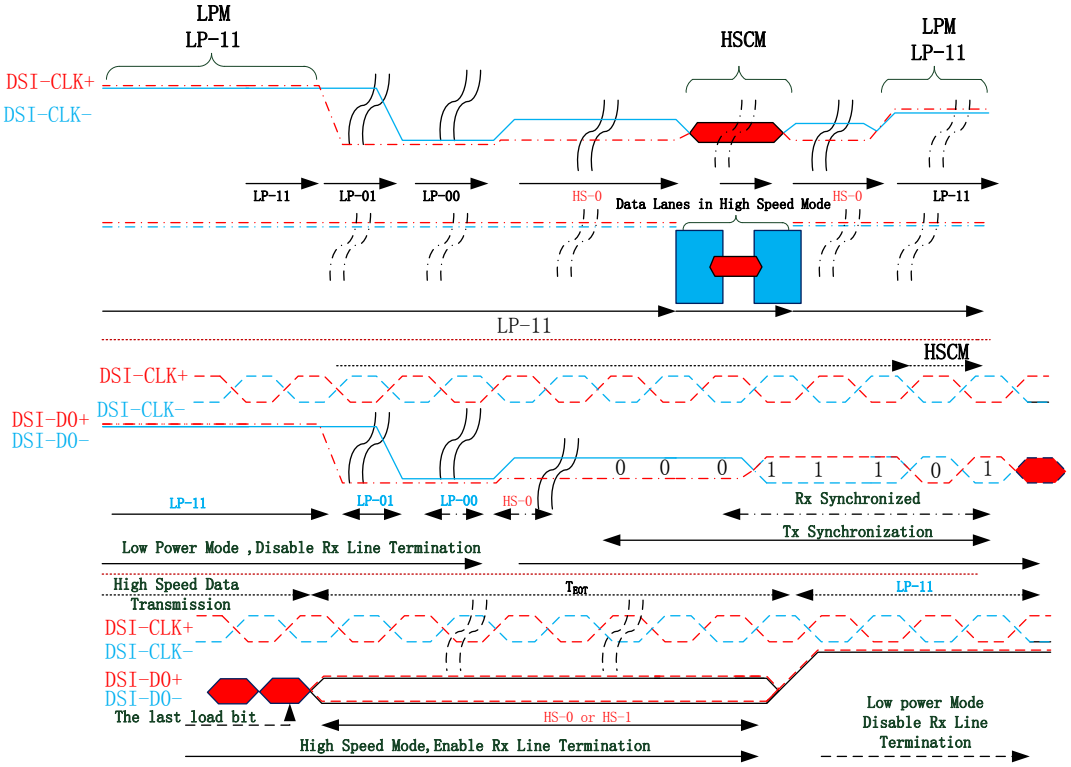


Figure: High speed clock burst

6.1.3 DSI data lanes

6.1.3.1 General

DSI-Dn+/- Data Lanes can be driven in different modes which are:
– Escape Mode (only support DSI_D0 data lane pair)
– High-Speed Data Transmission (support all data lane pairs)
– Bus Turnaround Request (only support DSI_D0 data lane pair)
These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	L P-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

6.1.3.2 Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward

direction and Reverse direction.

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Escape Command , which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.

• A payload stream if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. All currently available Escape mode commands and actions are list below.

• Send or receive “Low-Power Data Transmission” (LPDT)

• Drive data lanes to “Ultra-Low Power State” (ULPS)

• Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function)

• Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU,

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn’t match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state. For Data Lane1 and 2, only support ULPS Escape mode commands.

• Drive data lanes to “Ultra-Low Power State” (ULPS)

The basic construction is illustrated below:

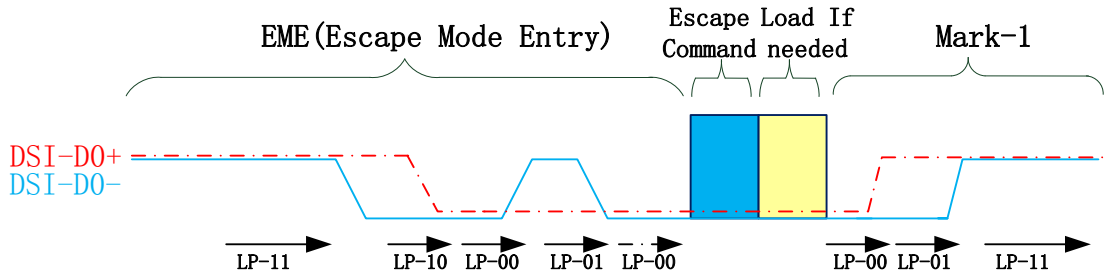


Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided 2 different groups: Mode or Trigger. Escape command groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin

Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode.

The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

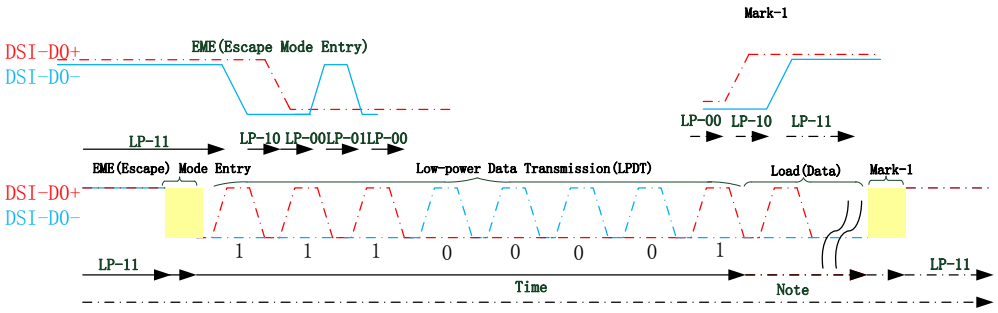
Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11
• Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
• Payload (Data):
- One or more bytes
- Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
• Mark-1: LP-00 =>LP-10 =>LP-11
• End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load(Data) is presenting the first bit is logical “1” in this example

Figure: Low-power data transmission

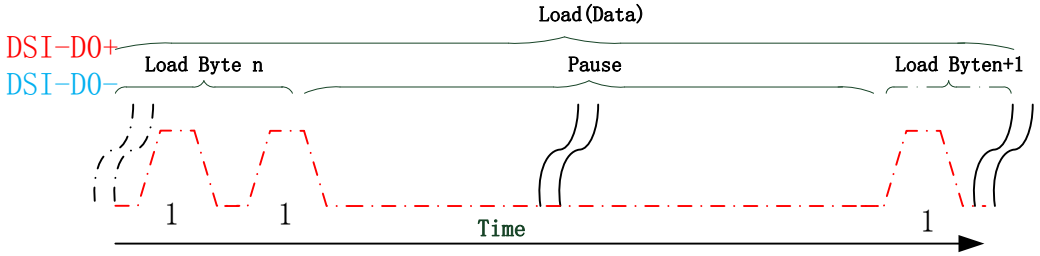


Figure: Pause (example)

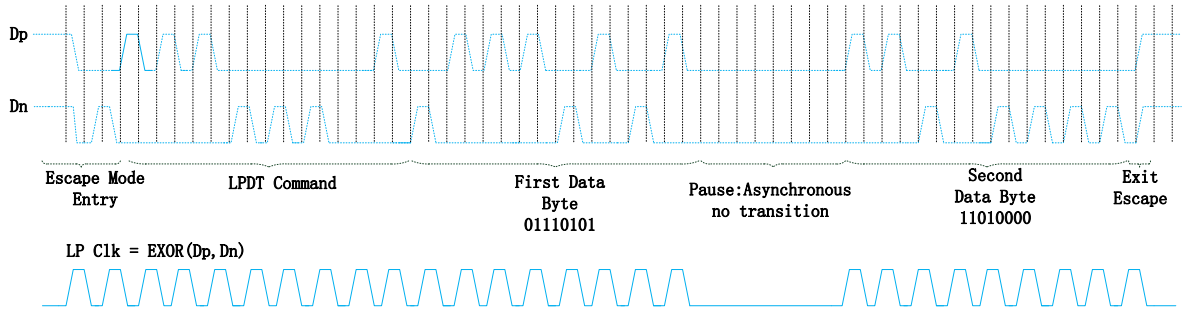


Figure: Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

• Start: LP-11
• Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
• Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
• Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
• Mark-1: LP-00 =>LP-10 =>LP-11
• End: LP-11

This sequence is illustrated for reference purposes below:

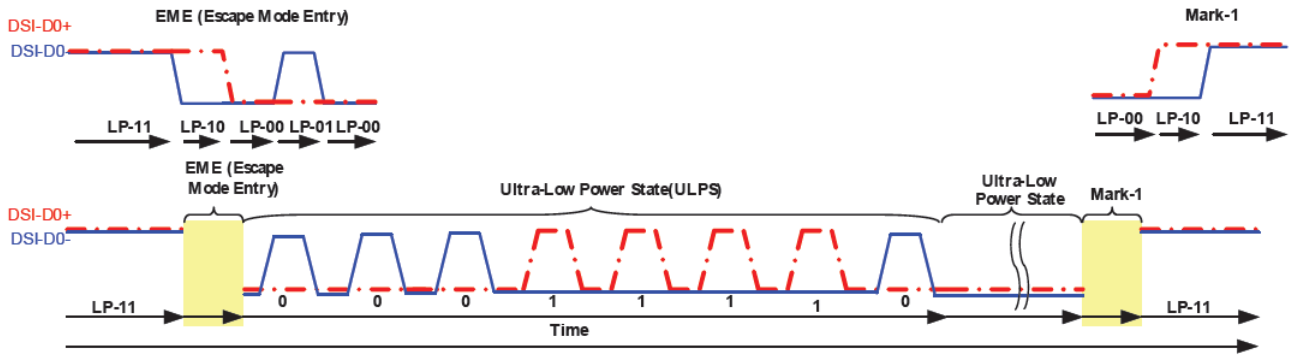


Figure: Ultra-low power state (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset is using a following sequence:

• Start: LP-11
• Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
• Mark-1: LP-00 =>LP-10 =>LP-11
• End: LP-11

This sequence is illustrated for reference purposes below:

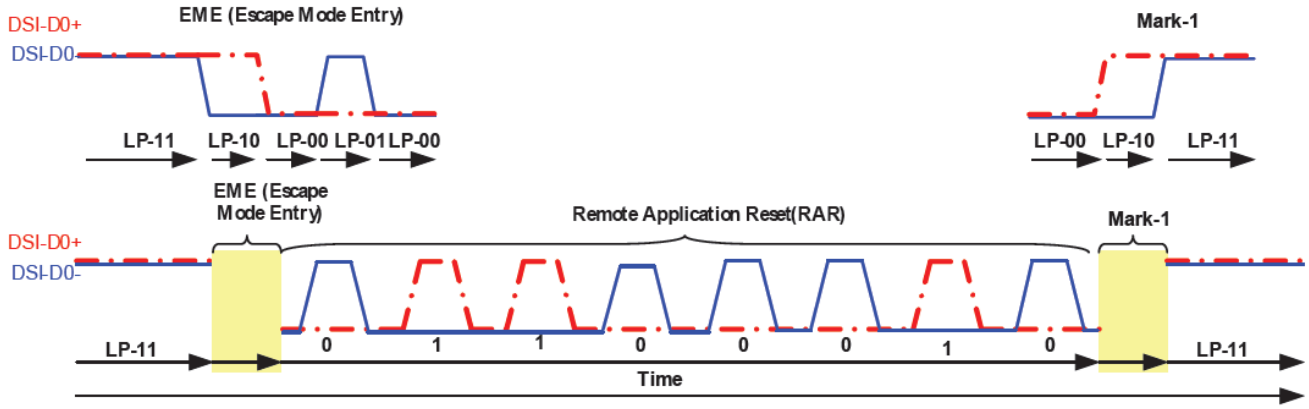


Figure: Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

• Start: LP-11
• Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
• Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
• Mark-1: LP-00 =>LP-10 =>LP-11
• End: LP-11

This sequence is illustrated for reference purposes below:

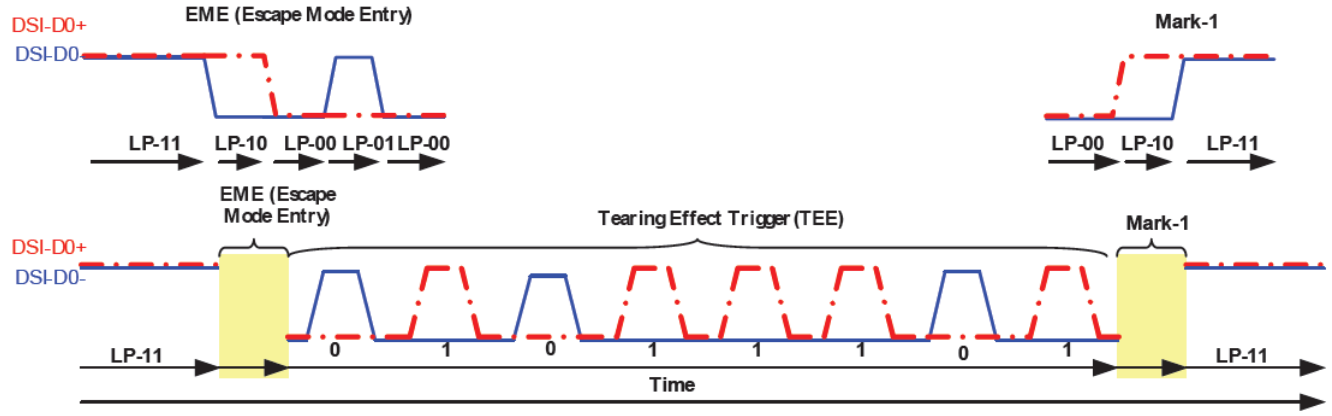


Figure: Tearing effect(TEE)

Acknowledgement (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11
• Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
• Mark-1: LP-00 =>LP-10 =>LP-11
• End: LP-11

This sequence is illustrated for reference purposes below:

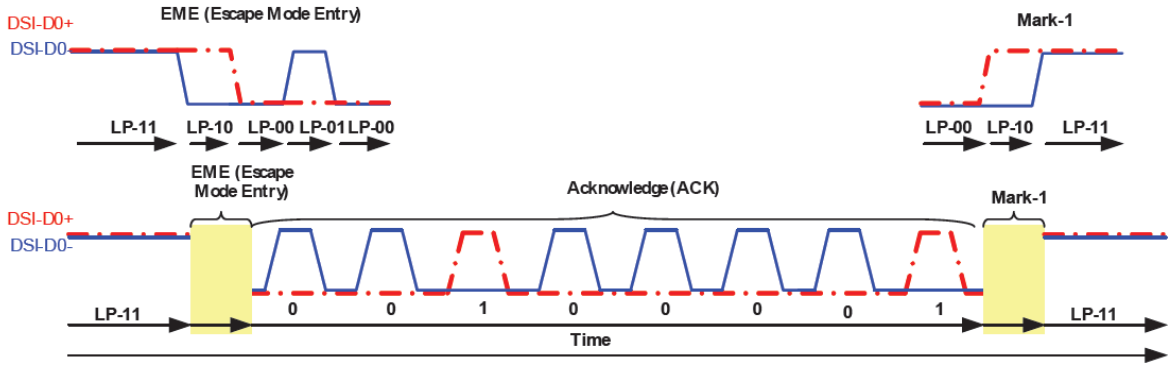


Figure: Acknowledgement (ACK)

6.1.3.3 High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (Tsot of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the HighSpeed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission(HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

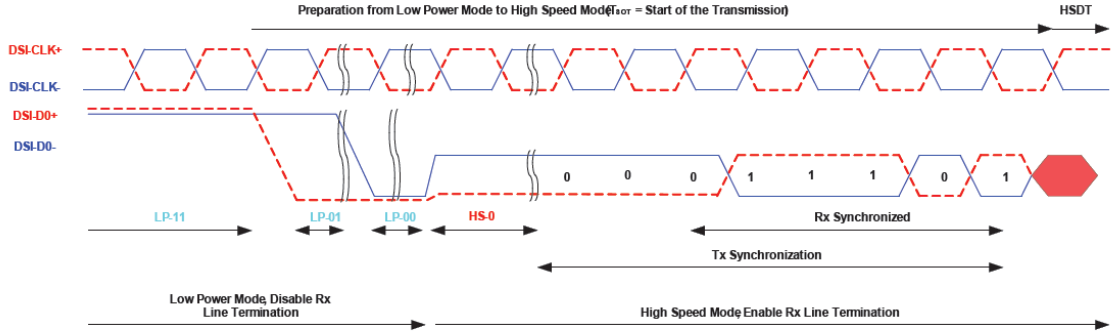


Figure: Tsot of HSDT

Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI- CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-D0+/- are in LP-11 mode. See more information on chapter “7.2.2 High-Speed Clock Mode (HSCM)”. Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

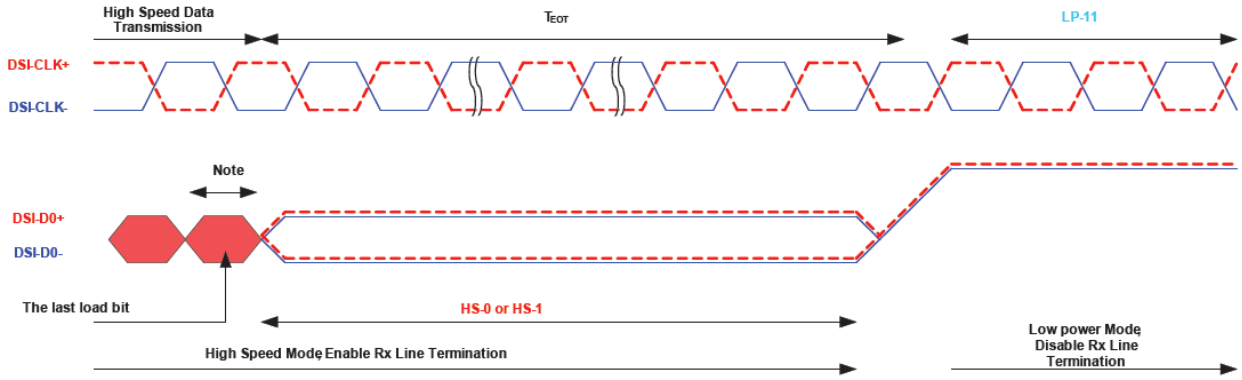
- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission

-MCU changes to HS-1, if the last load bit is HS-0

-MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below



Note:

If the last load bit is HS0, the transmitter changes from HS0 to HS-1.

If the last load bit is HS1, the transmitter changes from HS1 to HS-0.

Figure: TEOT of HSDT

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter "Short Packet (SPa) and Long Packet (LPa) Structures". These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

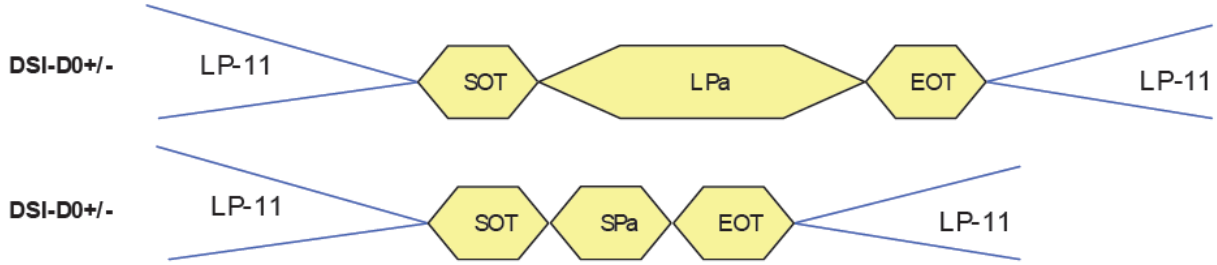


Figure: Single packet in HSDT

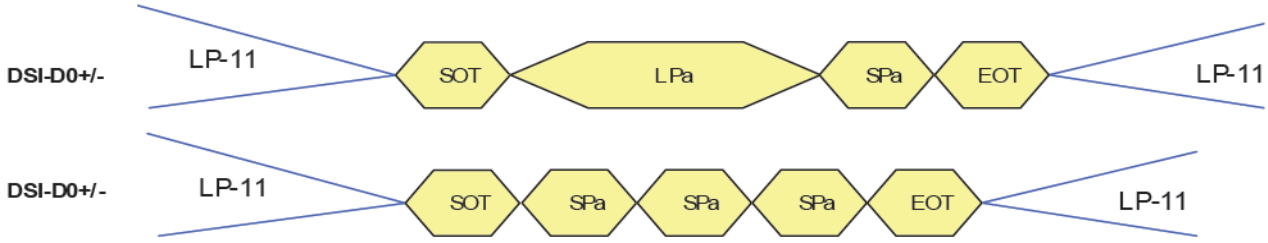


Figure: Multiple packets in HSDT

Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are ‘1’s (Stop Mode)
SOT	Start of the Transmission
LPa	Long Packet
SPa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

6.1.3.4 Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

• Start (MCU): LP-11

• Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00

• The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)

• The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.

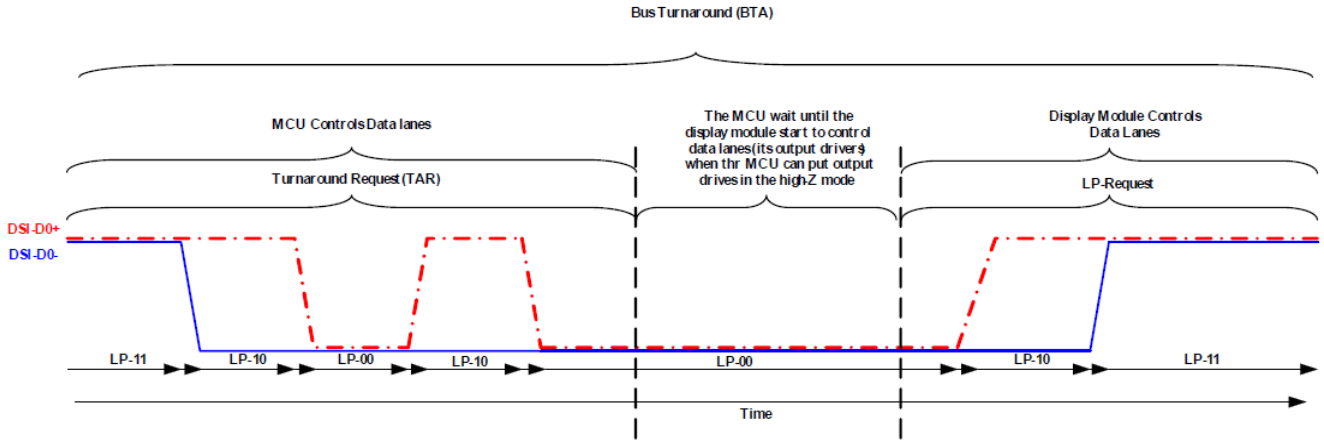


Figure: Bus turnaround procedure

6.1.3.5 Two Data-lane High Speed Transmission

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of lanes, one lane may run out of data before the other. Therefore, the lane management layer, as it buffers up the final set of less-than-2 bytes, de-asserts its “valid data” signal into all lanes for which there’s no further data. Although all lanes start simultaneously with parallel SoTs, each

operates independently and may complete the HS transmission before the other lane, sending an EoT one cycle (byte) earlier.

The two PHYs on the receiving end of the link collect bytes in parallel and feed them into the lane management layer. The lane management layer reconstructs the original sequence of bytes in the transmission. Figure 6.2.3.5.1 shows the way a HS transmission can terminate for two data-lane HS transmission.

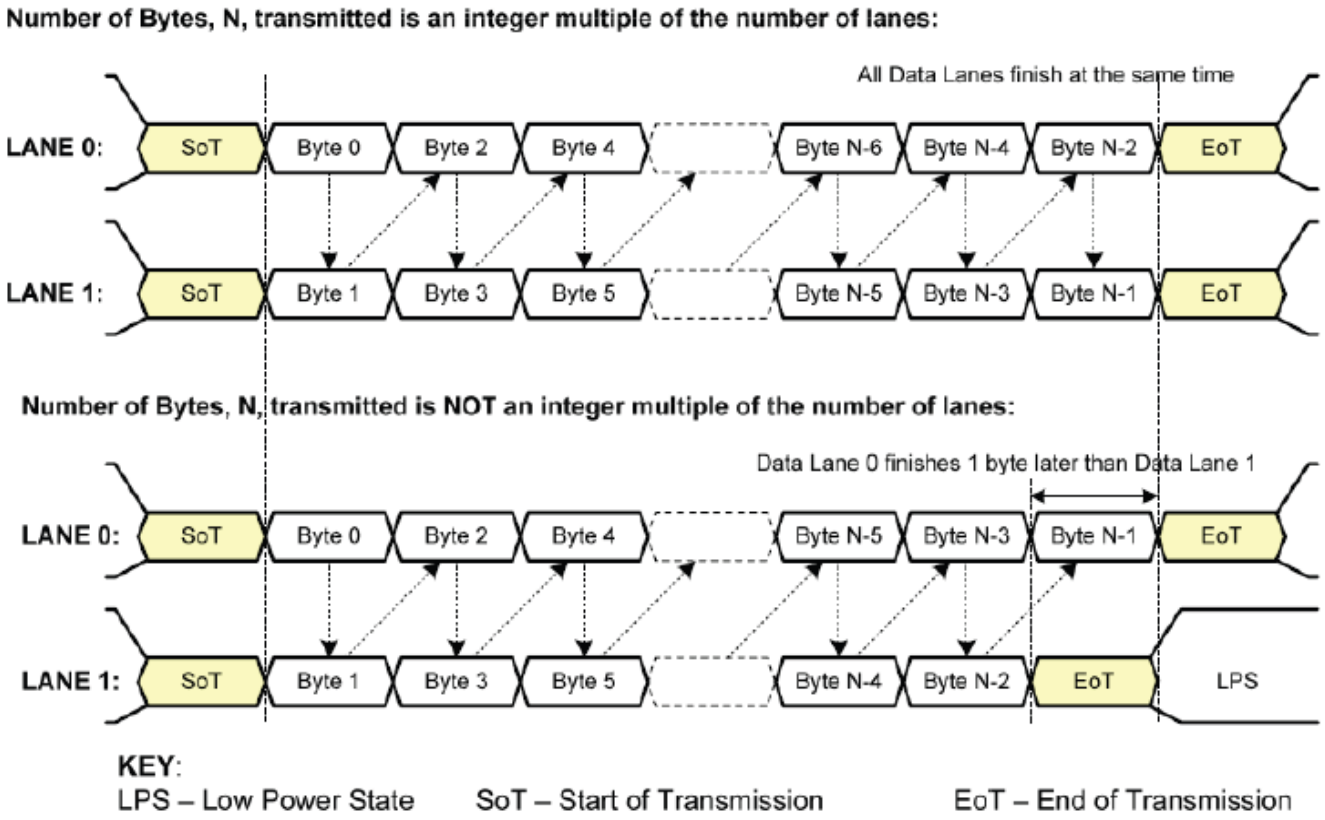


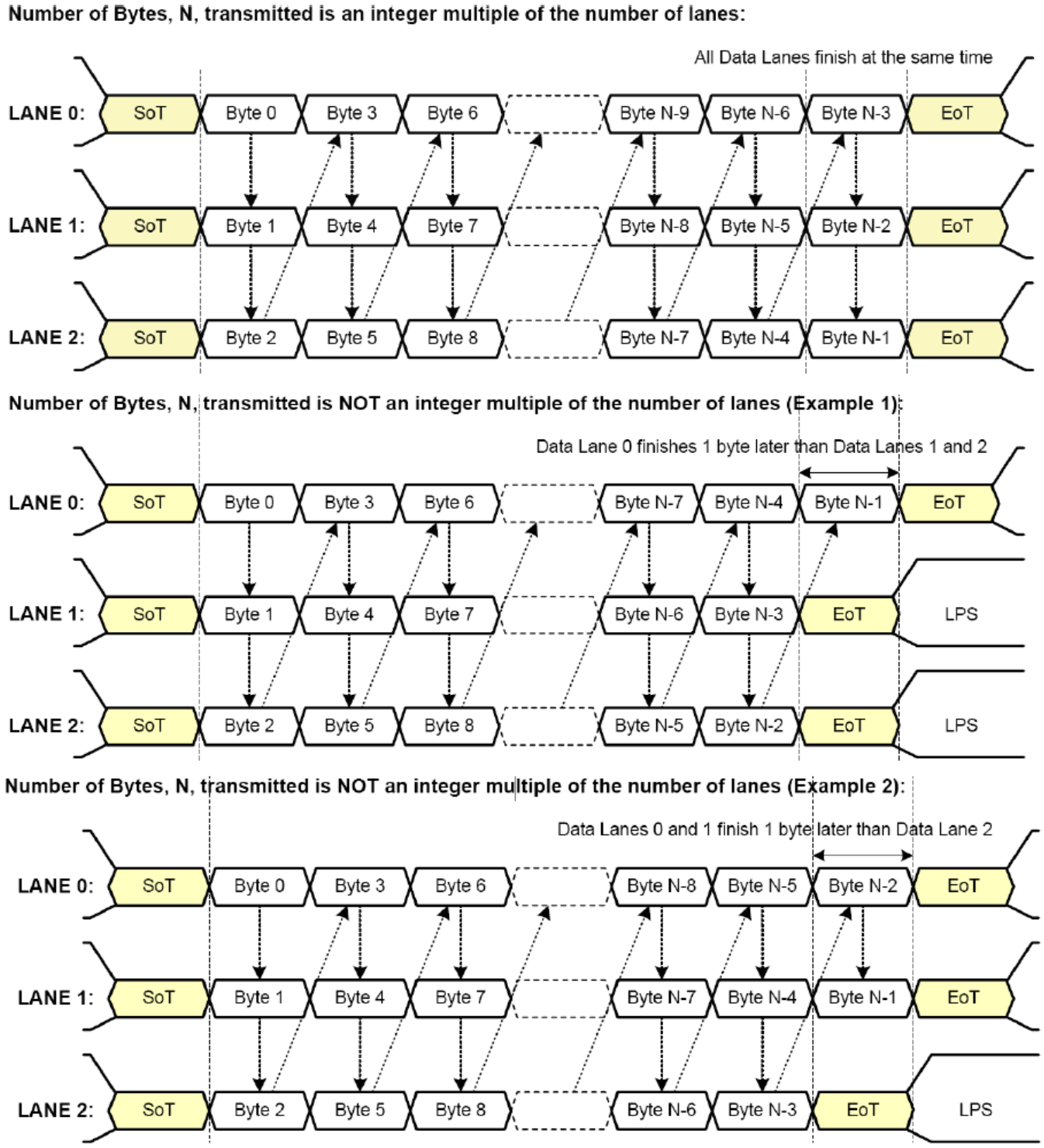
Figure: Two data-lane HS transmission example

6.1.3.6 Three data-lane high speed transmission

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier. The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission.

Below Figure illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.



6.1.4 Packet level communication

6.1.4.1 Short Packet (SPa) and Long Packet (LPa) structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

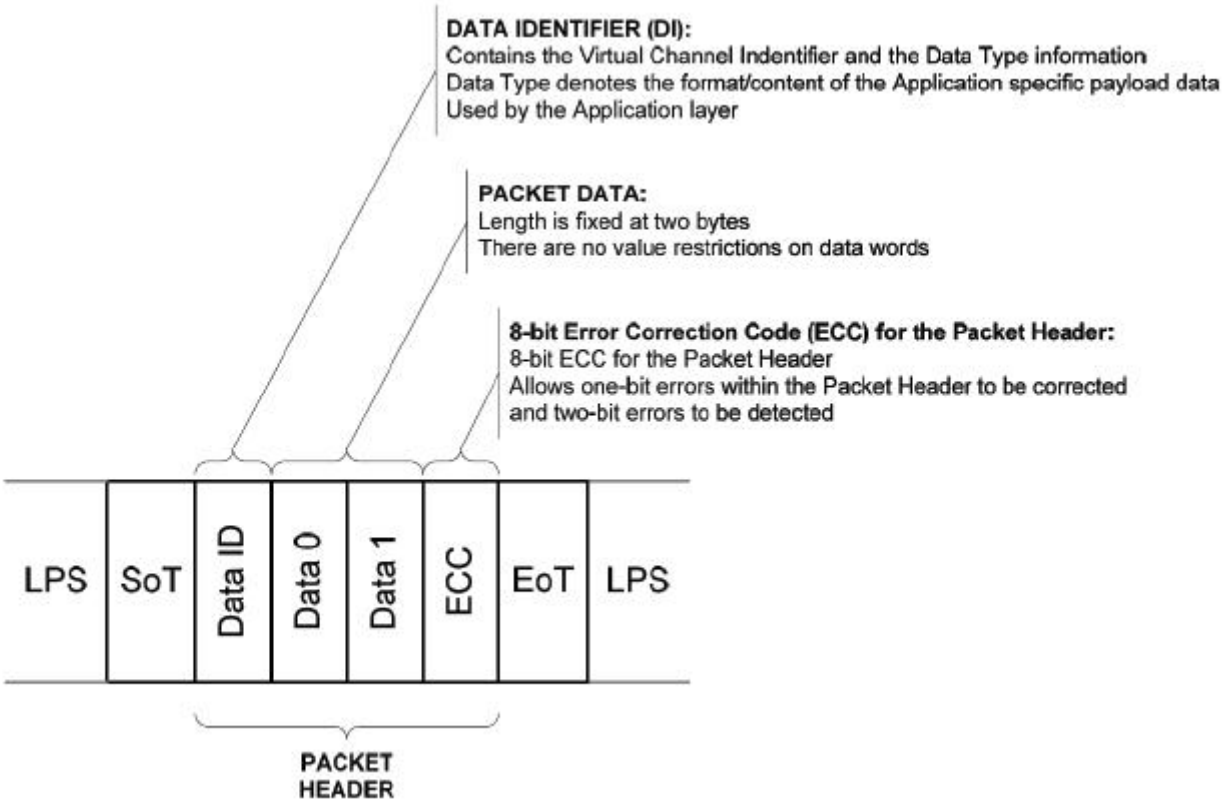


Figure: Short packet structure

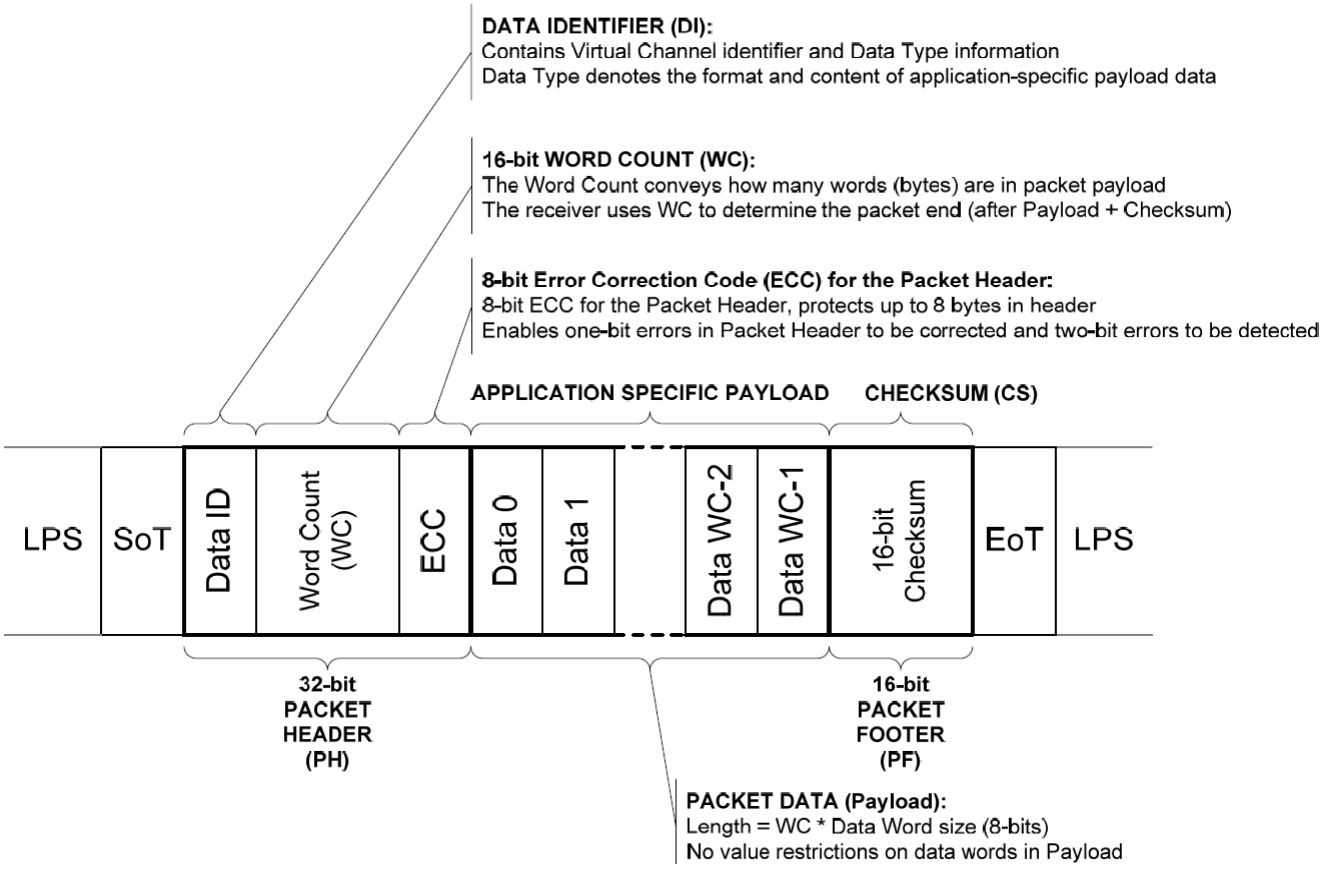


Figure:. Long packet structure

Note: Short Packet (SPa) Structure" and Long Packet (LPa) Structure" are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

- LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

Bit Order of the Byte on Packets

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure 6.2.4.1.3 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

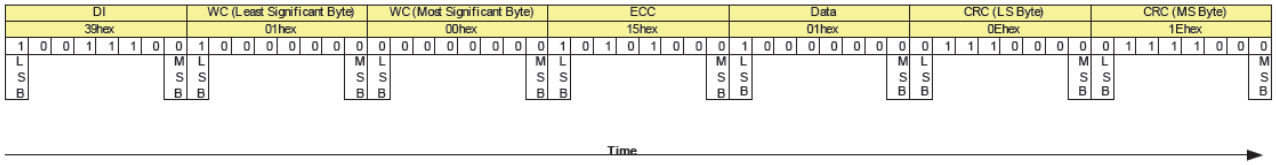


Figure: Bit order of the byte on packets

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last. e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

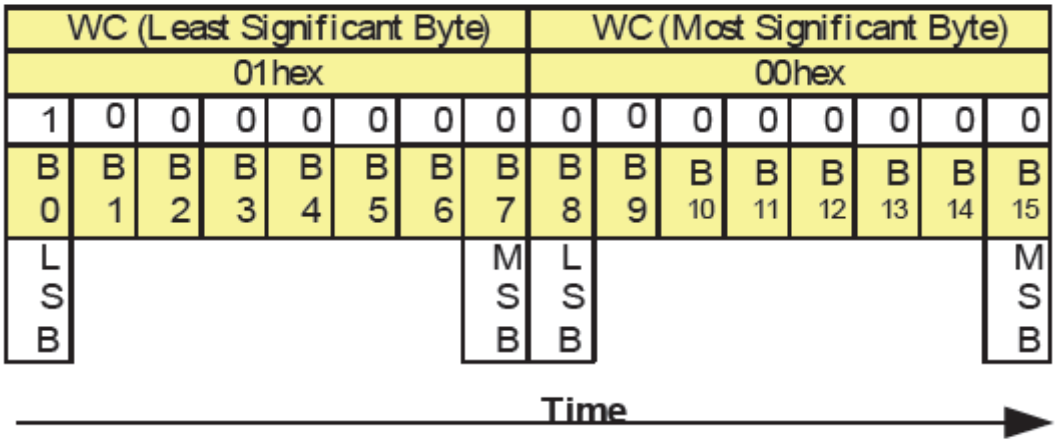


Figure: Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
• 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
• 4th byte: Error Correction Code (ECC)

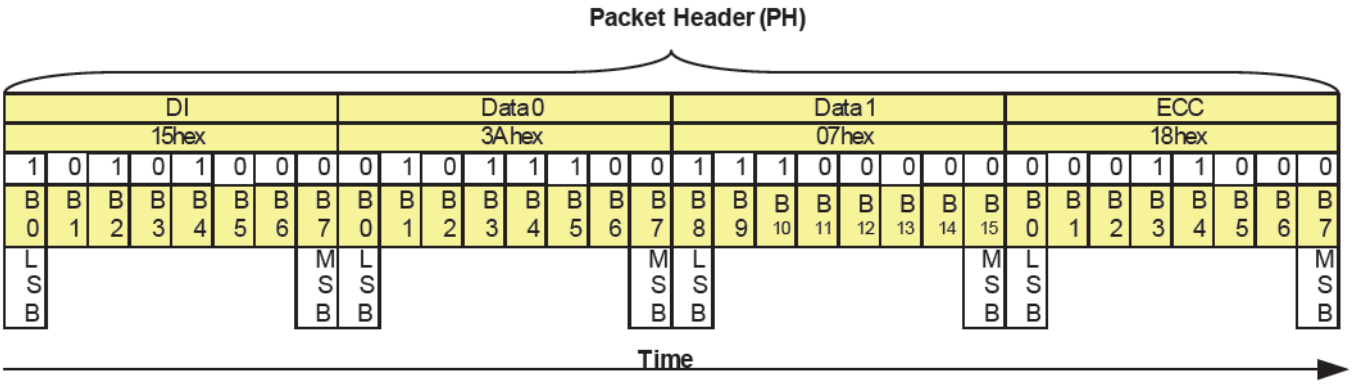


Figure: Packet head on short packet

Long Packet (LPa):
• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
• 2nd and 3rd bytes: Word Count (WC)
• 4th byte: Error Correction Code (ECC)

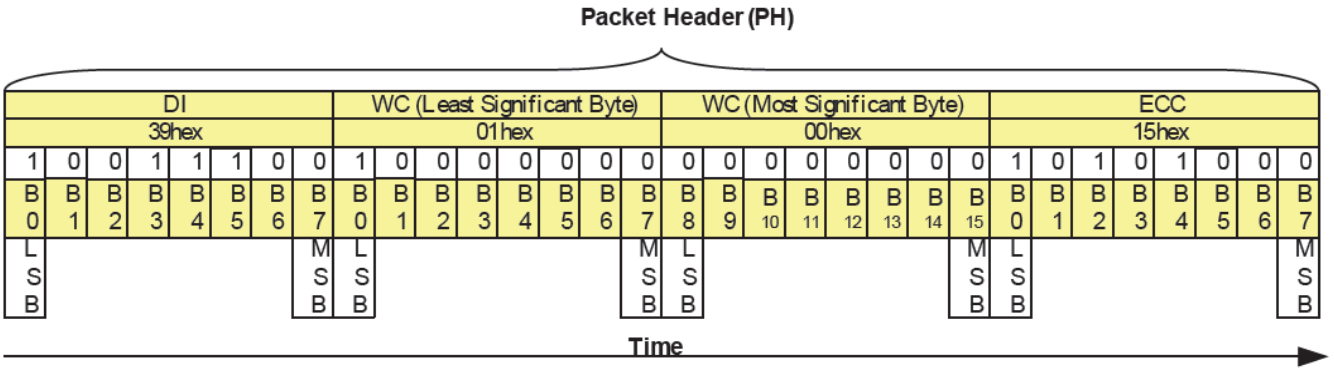


Figure: Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:
• Virtual Channel (VC), 2 bits, DI[7...6]
• Data Type (DT), 6 bits, DI[5…0]
The Data Identification (DI) structure is illustrated on a table below.

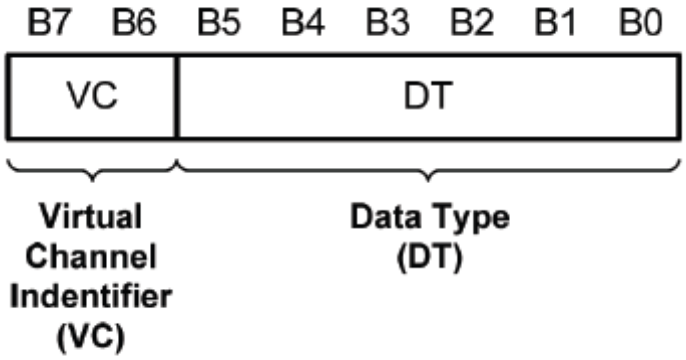


Table: Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

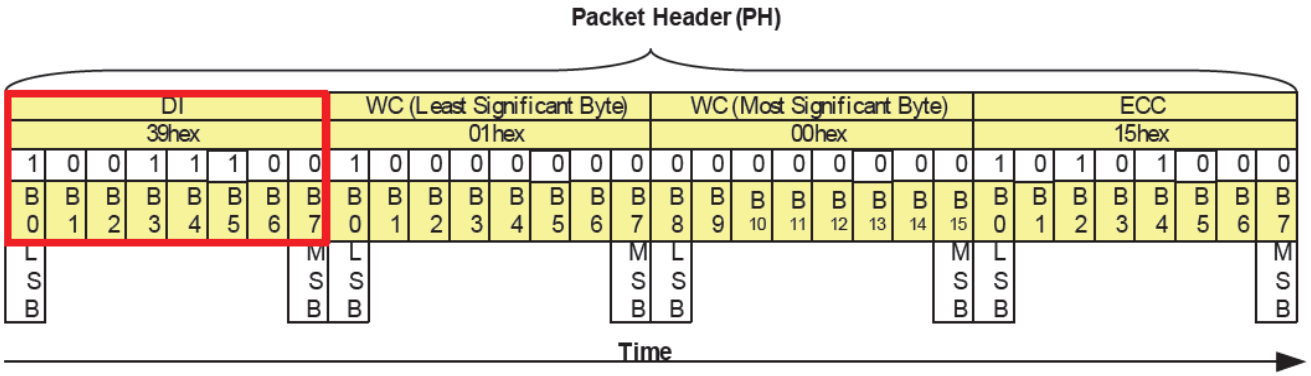


Figure: Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

OTM0000A only support VC code=00, package with other VC code(01/10/11) will be filter out.

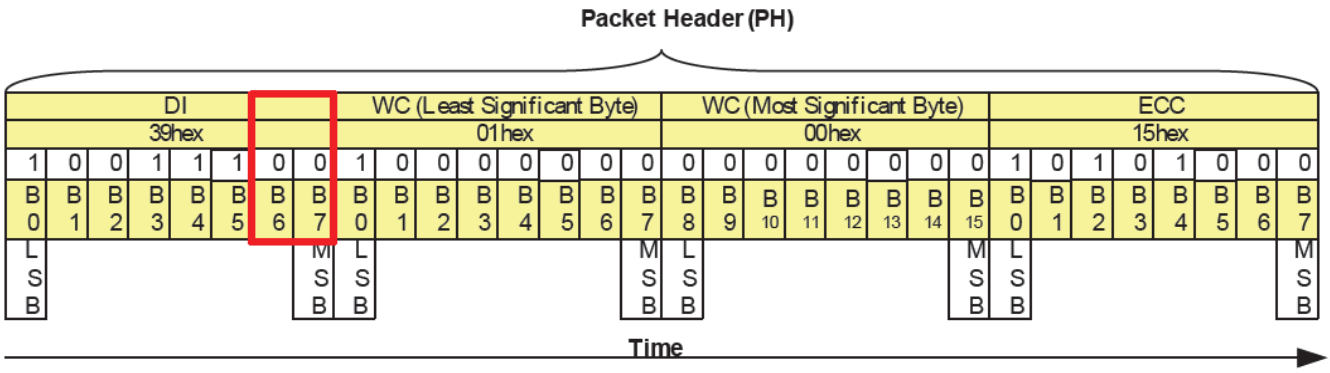


Figure: Virtual channel on the packet head

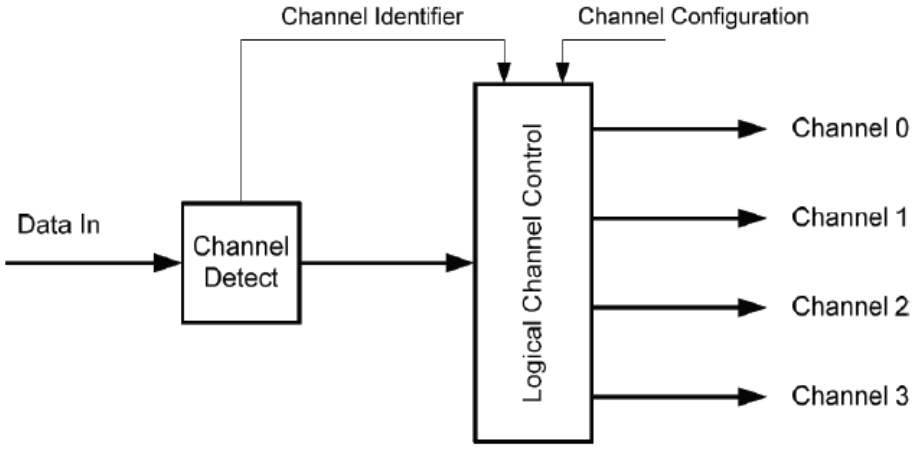


Figure: Virtual channel block diagram (receiver case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

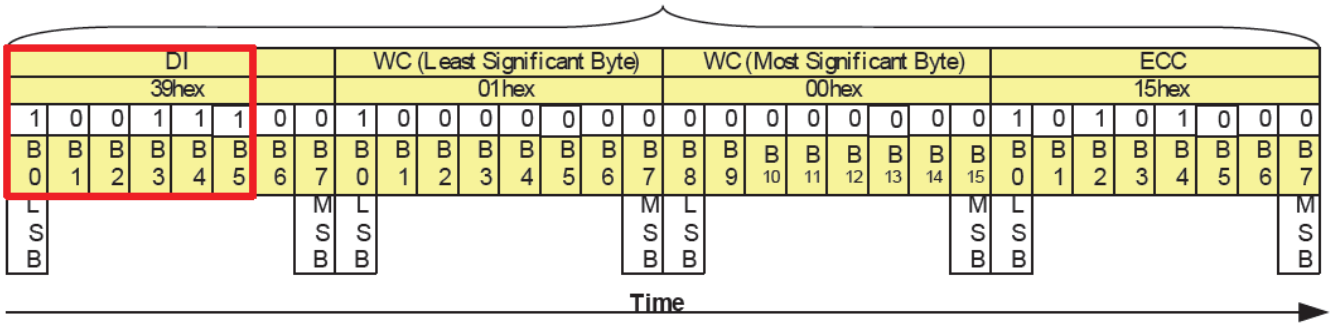


Figure: Data type on the packet head

The receiver is ignored other Data Type (DT) if they are not defined on tables above. Host send "Generic Read" data type, will return Generic Read package to Host.

Packet data on the short packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send. Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to 00h, if the information length is 1 byte. Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

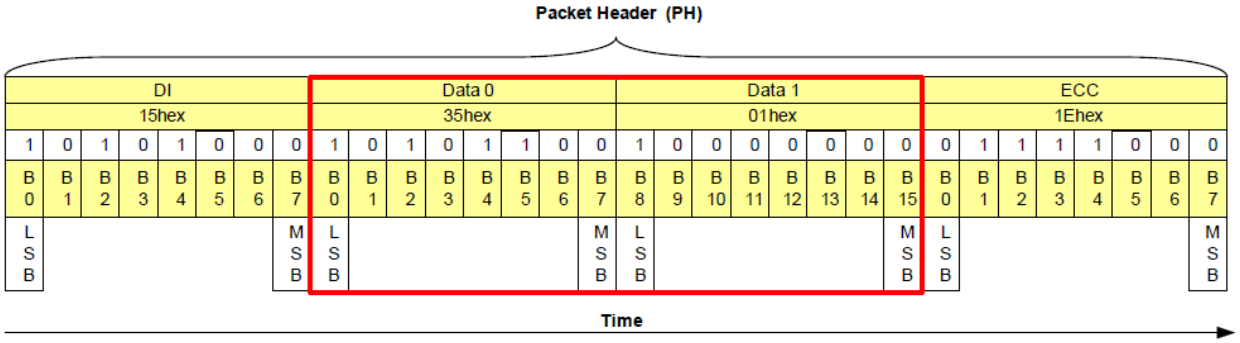


Figure: Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

• Data 0: 10hex

• Data 1: 00hex (Null)

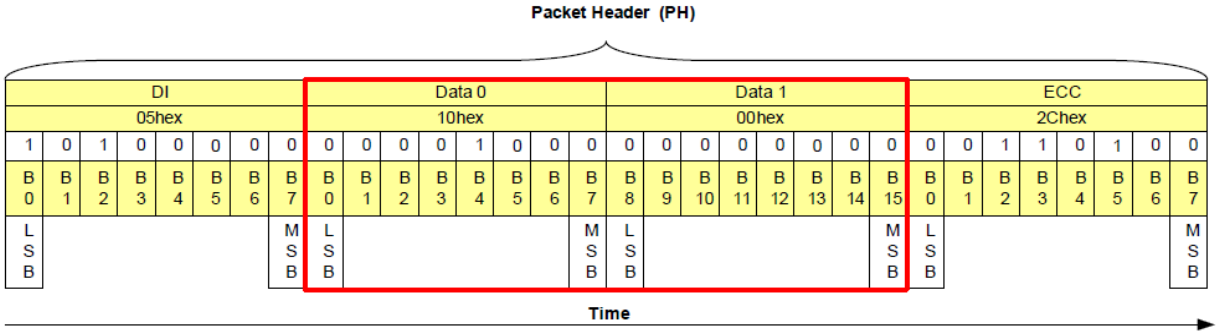


Figure: Packet data on the short packet, 1 bytes information

Word count on the long packet

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI)has indicated that Long Packet (LPa) is wanted to send. Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

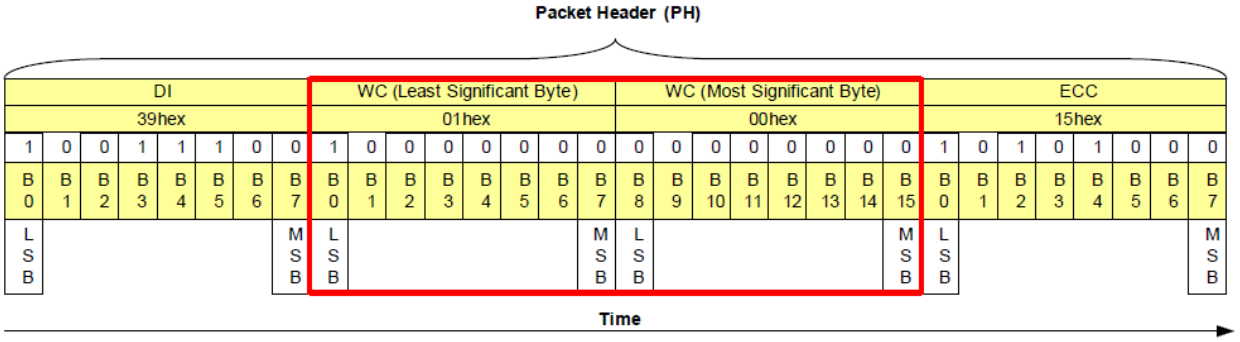


Figure: Word count on the long packet

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23…0])

D[23…0] is illustrated for reference purposes below.

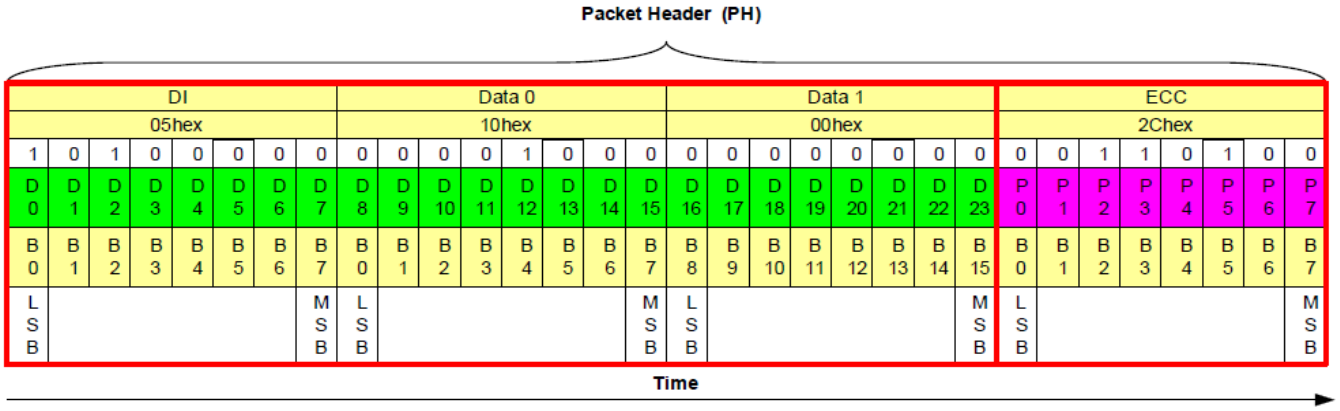


Figure: D[23:0] and P[7:0] on the short packet

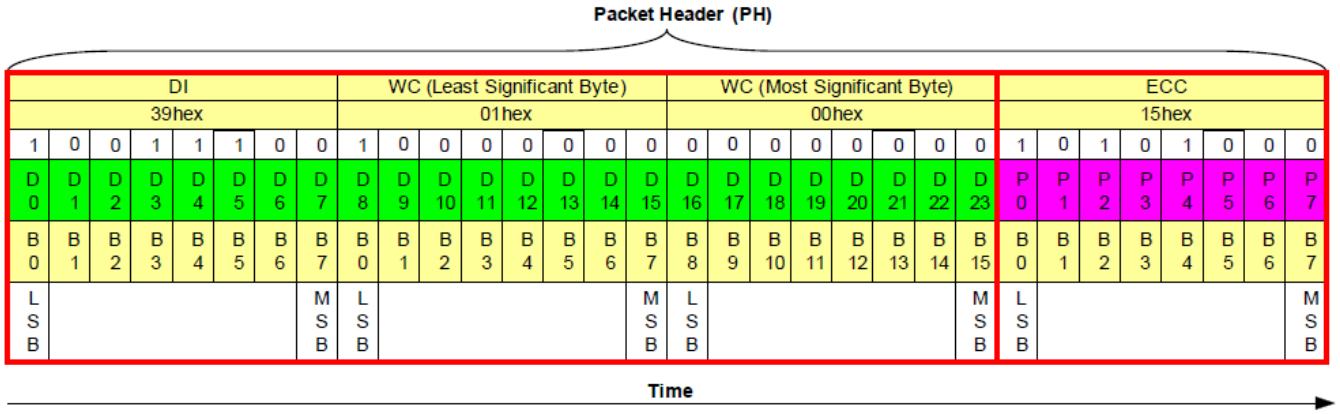


Figure: D[23:0] and P[7:0] on the long packet

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

ecc_parity = {P7,P6,P5,P4,P3,P2,P1,P0};

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

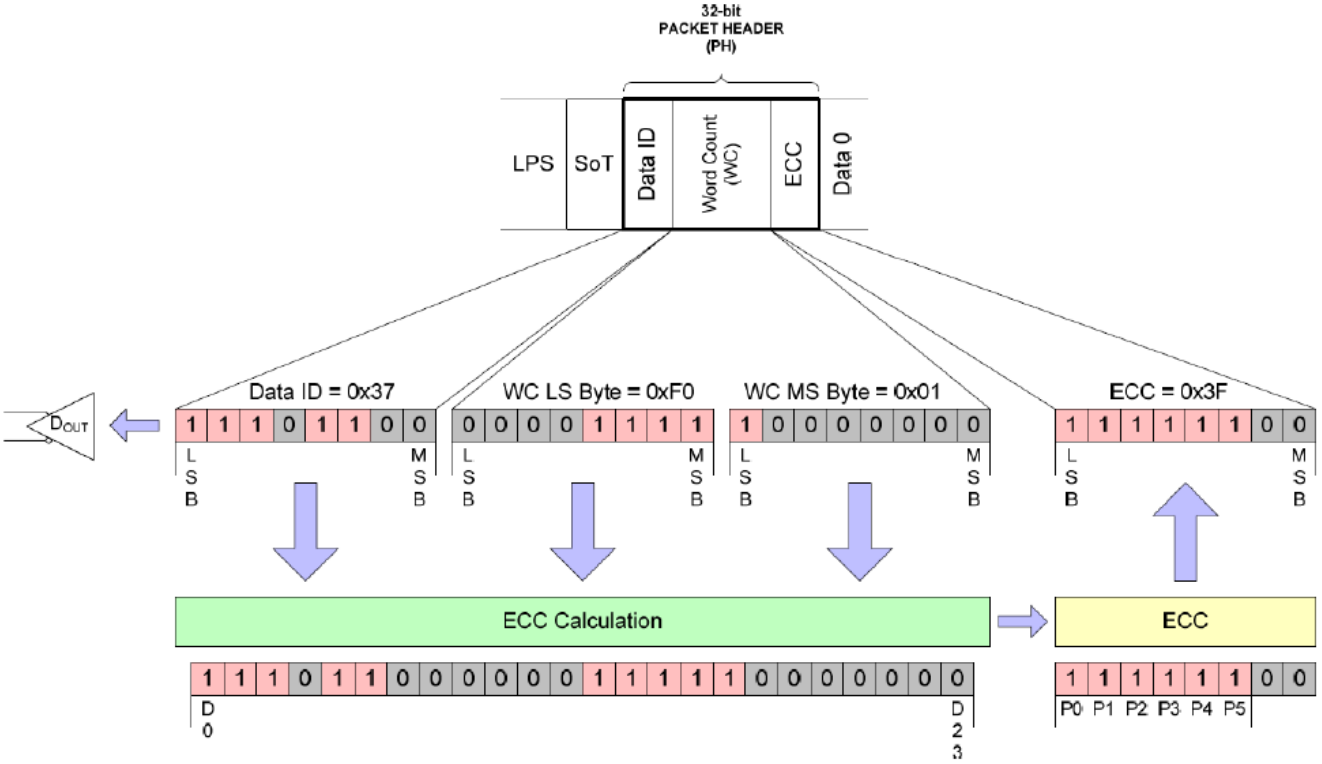


Figure: 24-bit ECC generation on TX side (Example)

Packet footer on the long packet

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

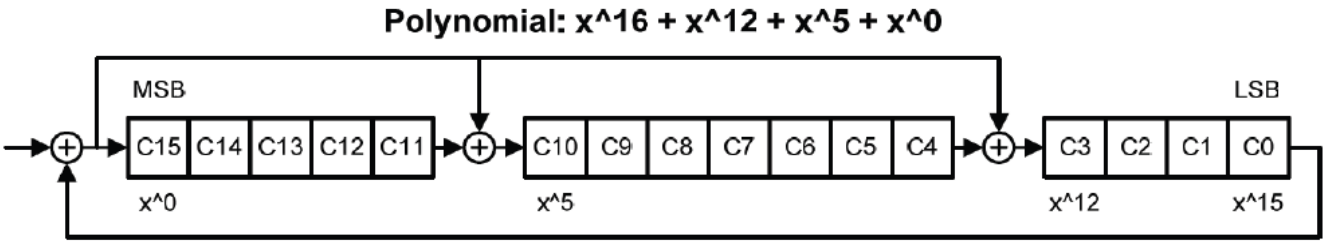


Figure: 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC). The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own

checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

6.1.4.2 Packet transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter "Instructions" is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

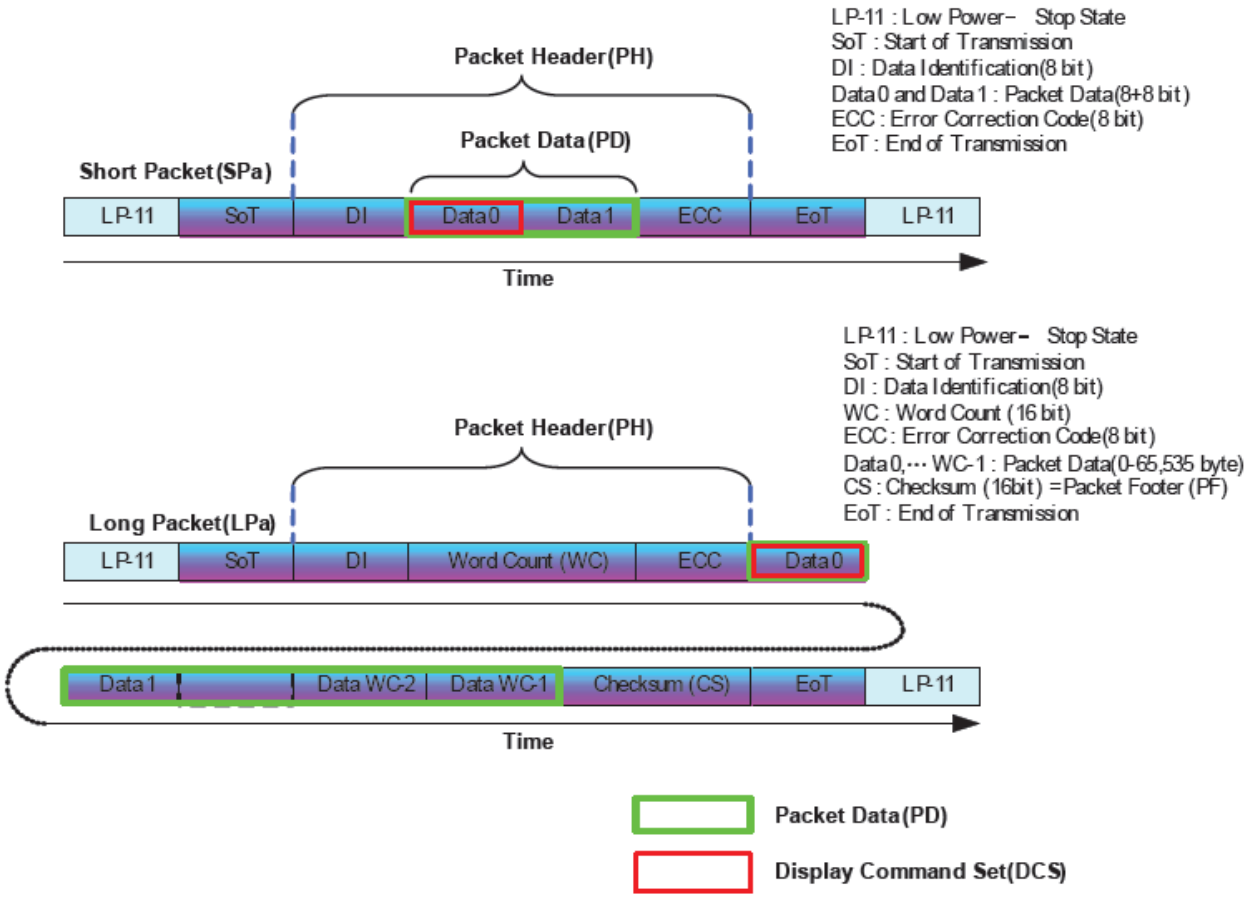


Figure: DCS on the short packet and long packet

Packet from the display module to the MCU

Used packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT).

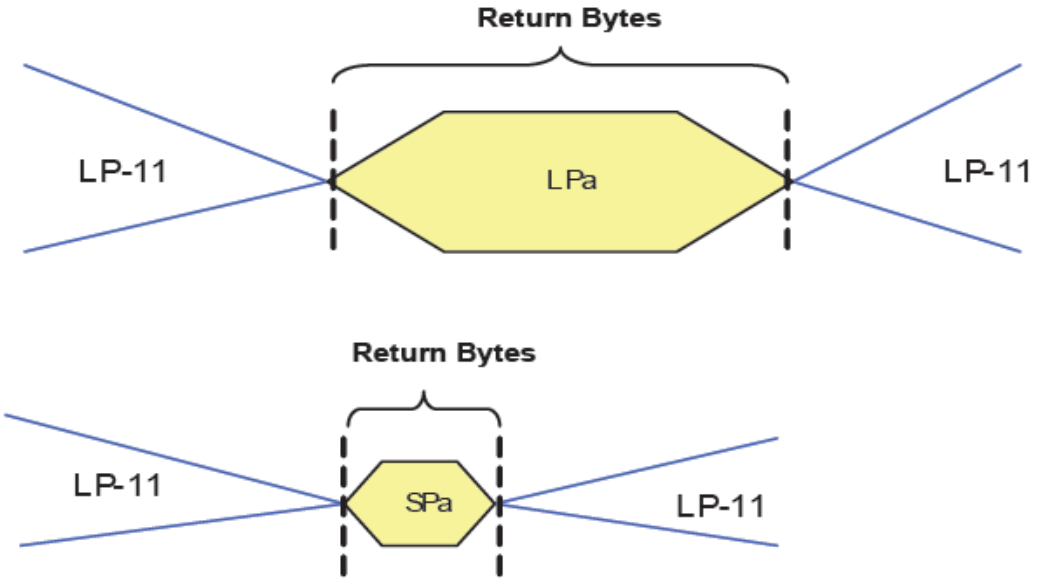


Figure: Return bytes on single packet

6.1.5 Customer-defined generic read data type format

The short packet of Data Type 14h (Generic READ, 1 parameters) specifies the register content for read and the Nth parameter that will begin reading. After Data Type 14h is received, BTA is executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

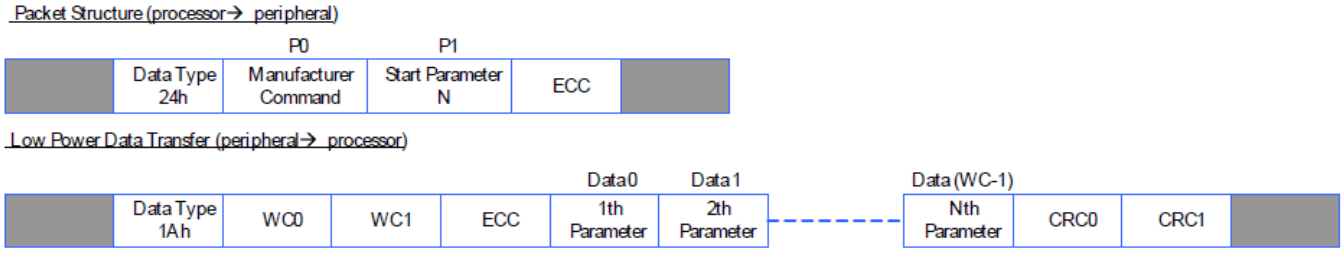


Figure: Generic read data type format

6.1.6 MIPI video parameter

In the MIPI video mode, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync (VS) indicates the beginning of each frame of the displayed image.

Hsync (HS) signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

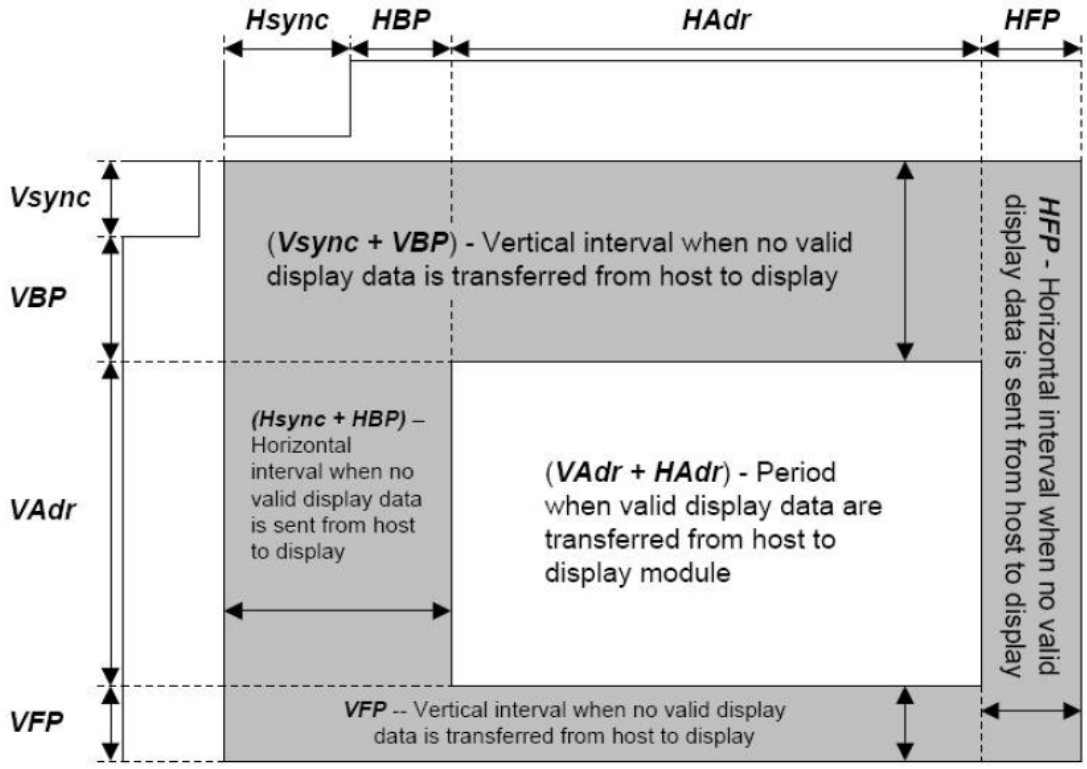


Figure 6.2.6.1 define timing parameter for MIPI video operation.

(Resolution for 750/720/640 horizontal x 1334 vertical display with Frame-Rate of 60 Hz)

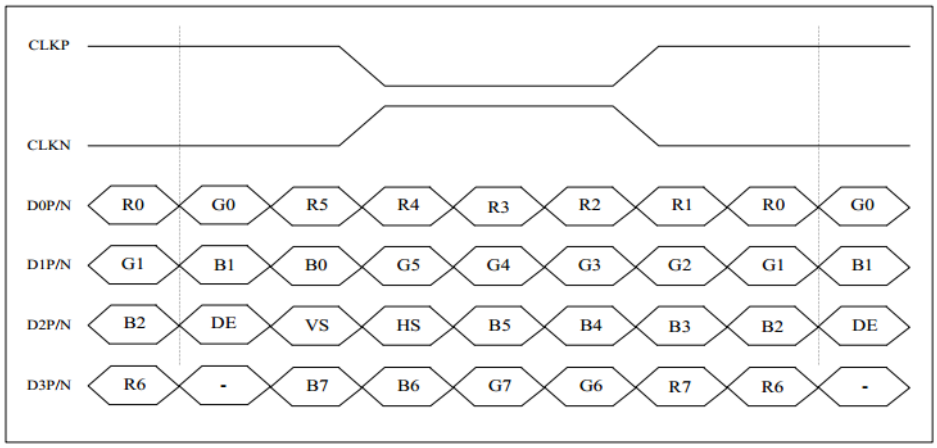
Parameters	Symbols	Min.	Typ	Max.	Unit
Horizontal Synchronization	Hsync	2	2	-	PCLK
Horizontal Back Porch	HBP	2	2	-	PCLK
Horizontal Front Porch	HFP	2	2	-	PCLK
Hsync+ HBP+ HFP	-	6	6	-	PCLK
Horizontal Address (Display area)	HAdr	-	720	-	PCLK

6.2 LVDS Interface

(Low-Voltage Differential Signals)
1 Channel LVDS Interface with 1 pixel / clock.
LVDS interface electrical specifications:

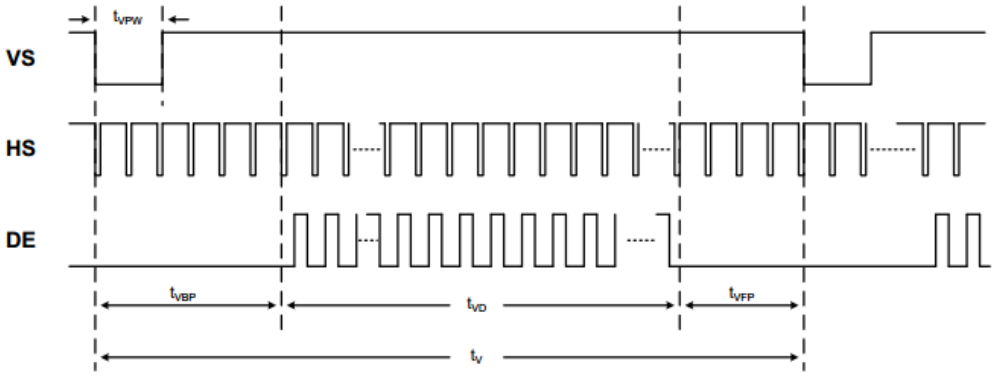
Parameter	**Symbol**	**Values**			**Unit**	**Notes**
		Min	**Typ**	**Max**		
Differential Input High Threshold Voltage	VLVTH	100	-	300	mV	
Differential Input Low Threshold Voltage	VLVTL	-300	-	-100	mV	

Common Input Voltage	VLVC	1	1.2	1.7-|Vid|/2	V	
Differential input voltage	|Vid|	0.2	-	0.6	-	

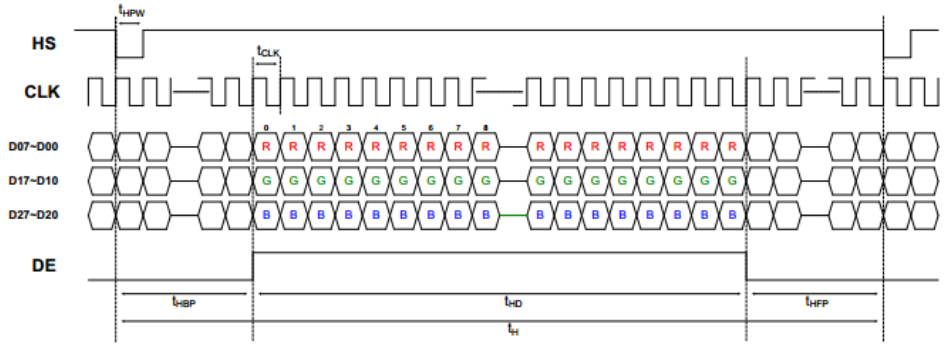


8-bit LVDS input(LVBIT=H, LVFMT=H)

Vertical input timing



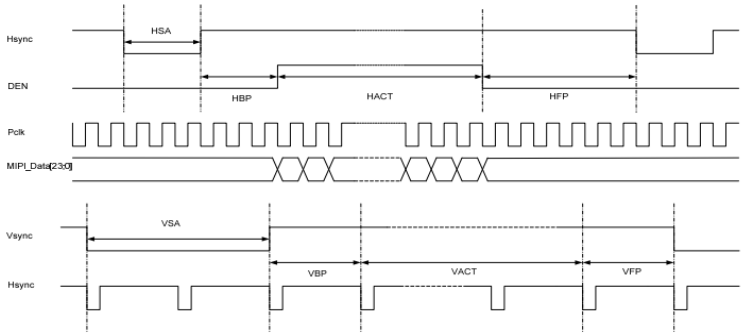
Horizontal input timing



6.3 RGB Interface

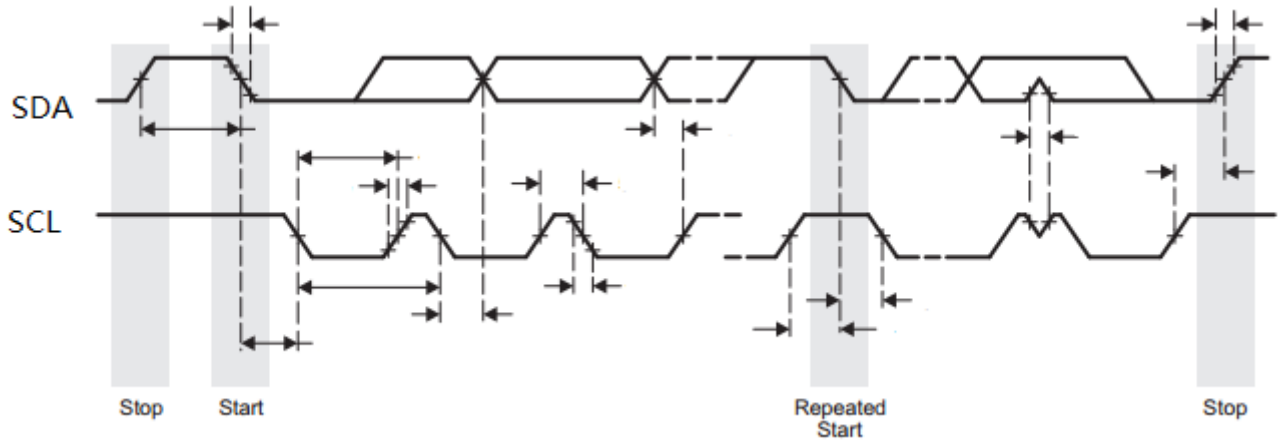
The RGB interface is used to provide display data for the video mode. The SPI interface is used to program the local registers of driver IC.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24bpp	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18bpp	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16bpp	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

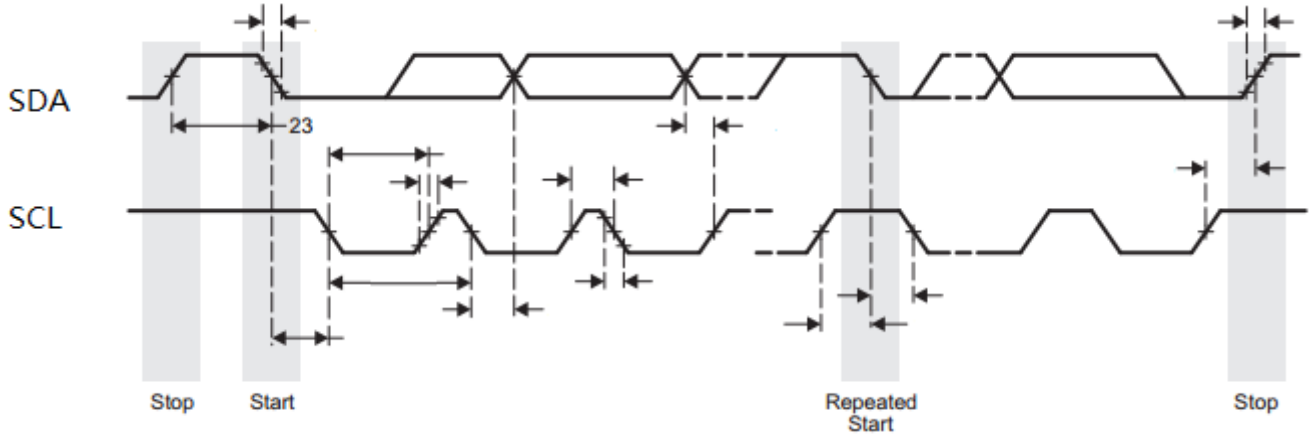


6.4 I2C Interface

Inter-Integrated Circuit provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module.



I2C Receive Timing



I2C Transmit Timing

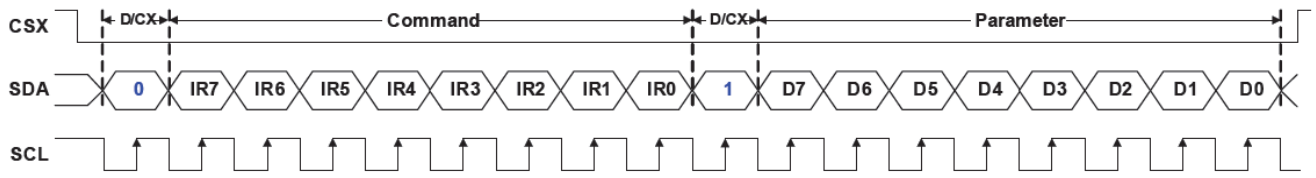
6.5 SPI Interface

The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

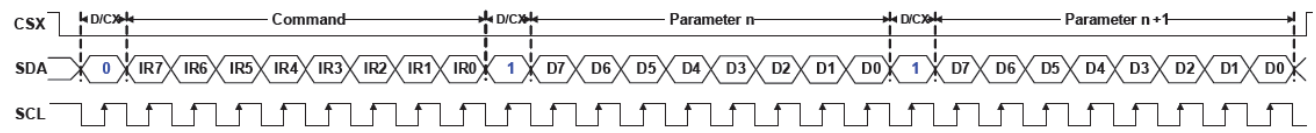
6.5.1 SPI write mode

The write mode of the interface means the micro controller writes commands and data to the Y13 . The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low. SDI / SDO is sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

Register Write: Singal Parameter



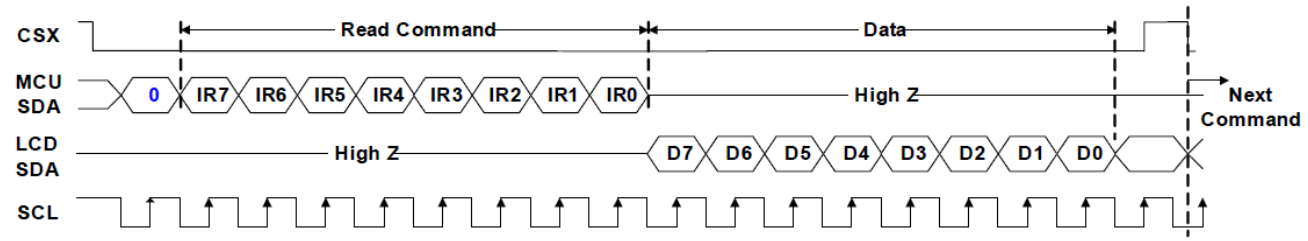
Register Write: Multiple Parameters



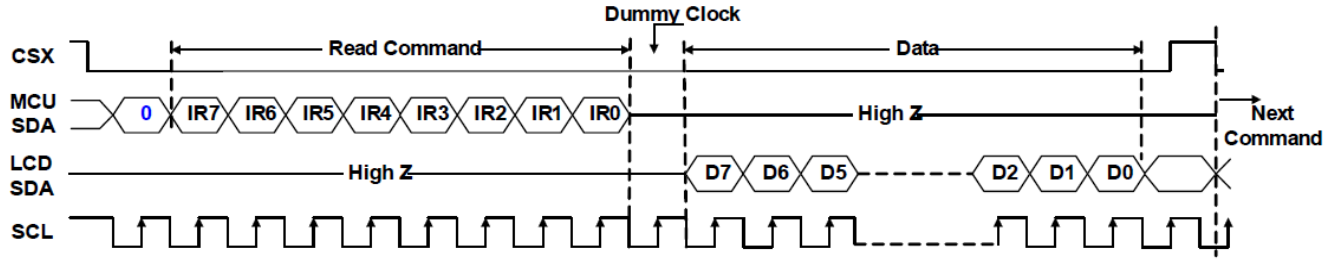
6.5.2 SPI read mode

The read mode of the interface means that the micro controller reads register value from the Y1 . To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send. The Y1 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. For the memory data read, a dummy clock cycle is needed (8 SCL clocks) to wait the memory data send out in SPI interface. But it doesn't need any dummy clock when execute the command data read.

Register Read: Without dummy clock



Register Read: With dummy clock



6.6 Power On/Off Sequence

IOVCC and VSP can be applied in any order. IOVCC and VSP can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VSP and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VSP can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

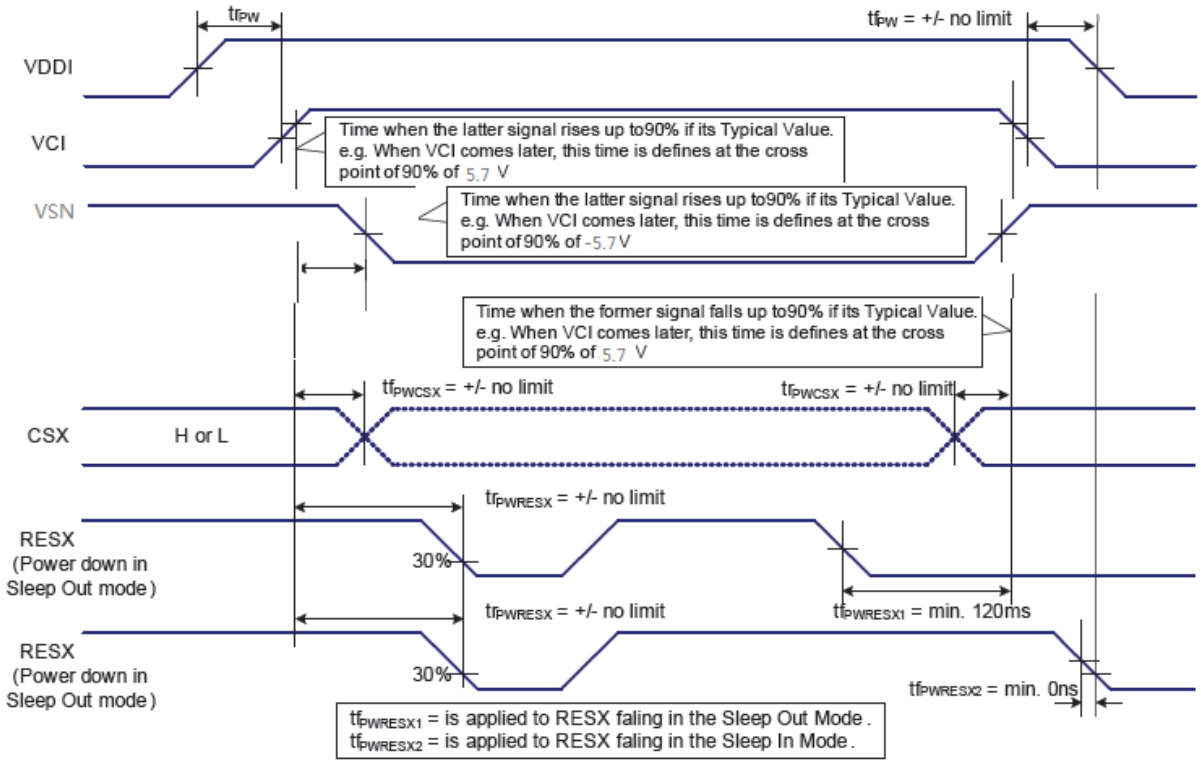
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.

Also between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

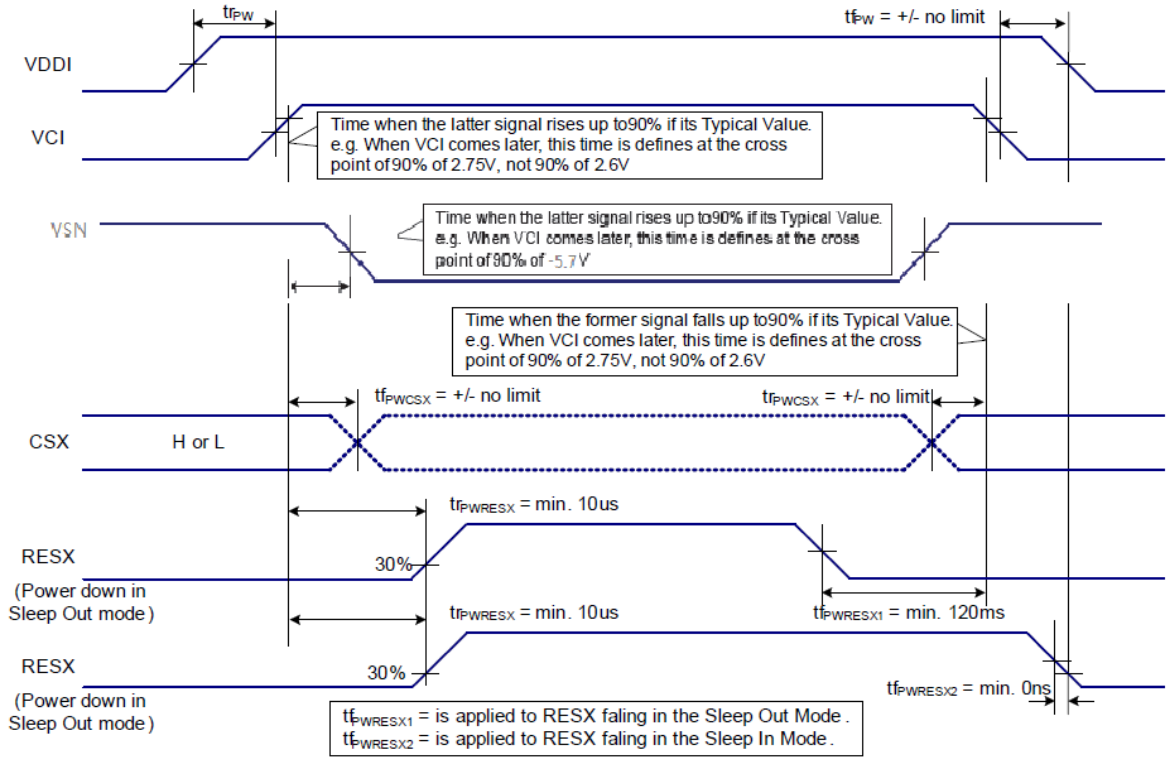
6.6.1 Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VSP and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



6.6.2 Case 2 – RESX line is held low or unstable by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10sec after both VSP and IOVCC have been applied.



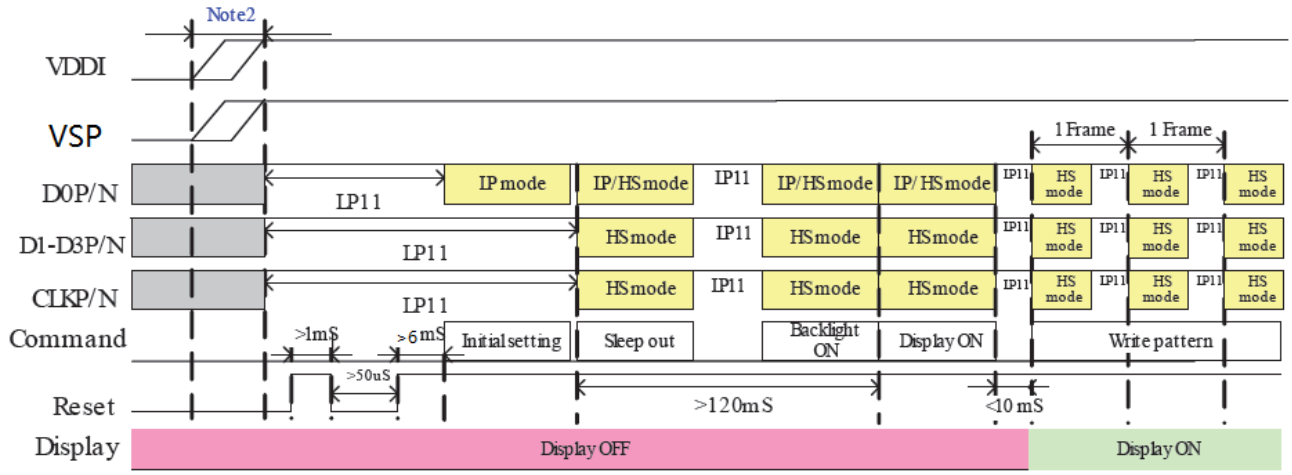
6.6.3 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

6.6.4 Power-on/off sequence for MIPI interface

The following diagram is including the power ON/OFF sequence for
(1). Two power mode (IOVCC, VSP) (2). Three power mode (IOVCC, VSP, VSN)

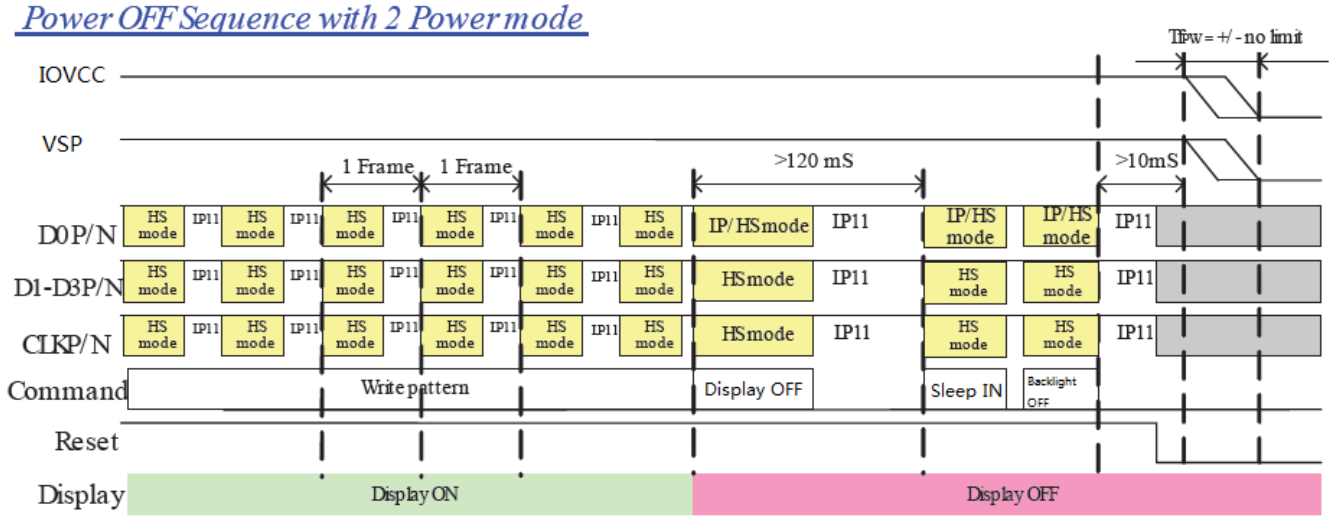
Power ON Sequence with 2 Power mode



Note :

1. Propose using non-continuous CLKwith Burst mode
2. wer ON/OFFSequence with 3 Power mode (External IOVCC, VSP, VSN)
3. Unless C1,the rest can be sent with HS/LPmode

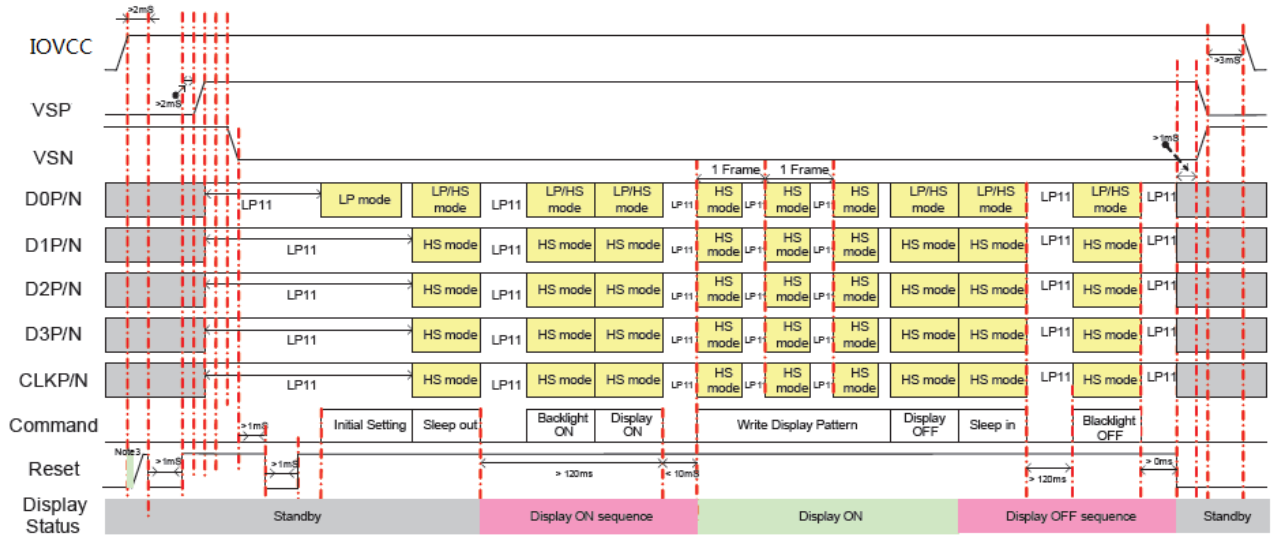
Power OFF Sequence with 2 Power mode



Note :

1. Propose using non-continuous CLK with Burst mode
2. 3.Unless C1,the rest can be sent with HS/LPmode

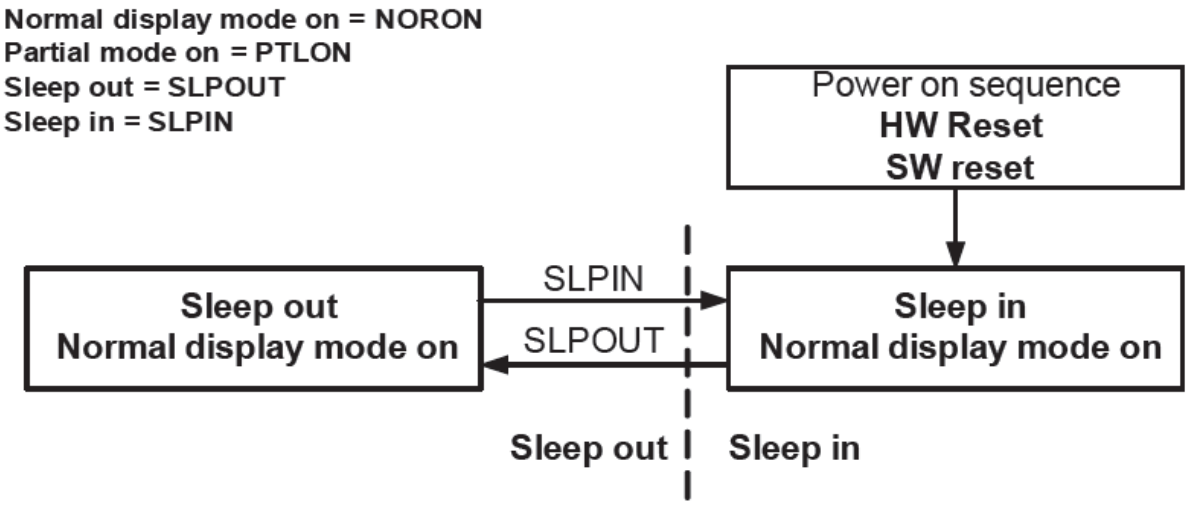
Power ON/OFF Sequence with 3 Power mode (External VDDI, VSP, VSN)



Note :

1. Propose using non-continuous CLKwith Burst mode
2. For IOVCC, VSP, VSN power, propose applying them separately and having 10 ms timing gap
3. Propose keeping Reset=Low when applying IOVCC
4. Unless C1,the rest can be sent with HS/LPmode

6.7 Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

6.8 Tear Effect Information

6.8.1 General

The MCU is updating the frame memory of the display module via its interface (DSI).
The display module is refreshing the display panel from the frame memory independently and it does not know what is happening on the interface of the display module (The MCU is sending image information to the display module). It is possible that this asynchronous updating is causing an abnormal visual effect on the display panel of the display module. Therefore, the display module is sending a synchronous information (= Tearing Effect Information), which is telling the position of the refreshing on the display panel, to the MCU which can decide when it can send image information to the display module (Mainly used for a moving image e.g. video clips) that there can avoid the abnormal visual effect on the display panel of the display module.

This Tearing Effect information can be sent in two different ways:

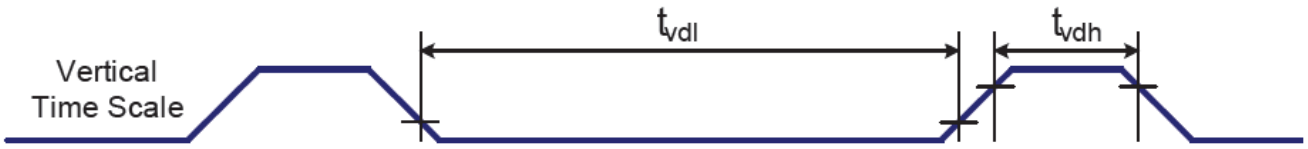
• Separated Line, which is so-called Tearing Effect (TE) line

• Bus, which is so-called Tearing Effect (TEE) Bus Trigger, when the display module is sending a trigger to the MCU The TE line can be used in DSI case if the Tearing Effect (TEE) bus trigger is not possible to use and the Tearing Effect (TEE) Bus Trigger is only used in DSI case.

6.8.2 Tearing effect line models

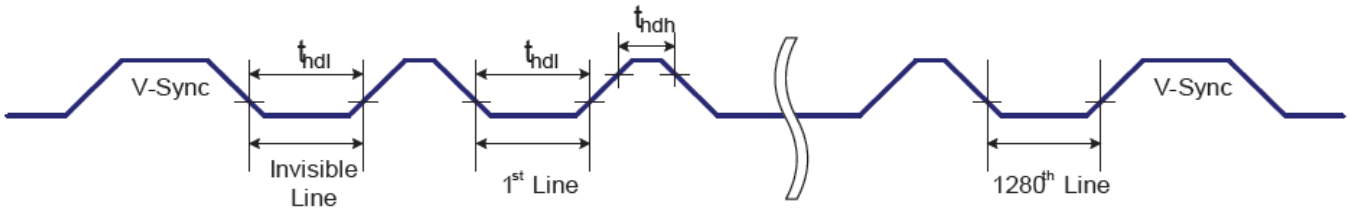
The Tearing Effect line supplies to the MCU a Panel synchronisation signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.

Mode 1：The Tearing Effect Output signal consists of V-Sync information only:

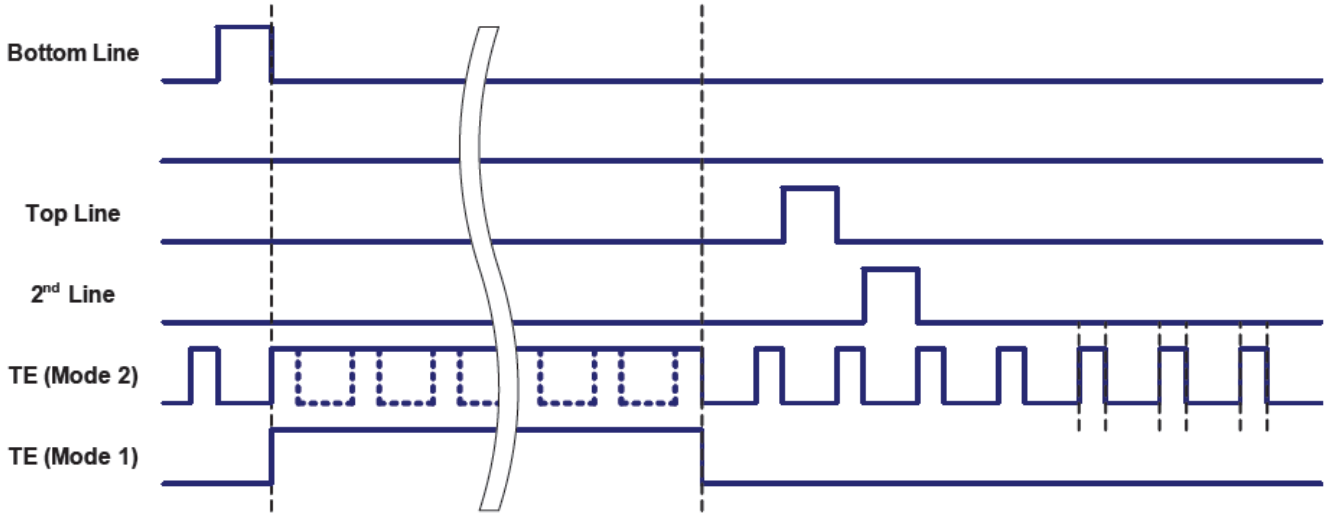


tvdh = The display panel is not updated from the Frame Memory.
tvdl = The display panel is updated from the Frame Memory (except Invisible Line – see below).

Mode 2：The Tearing Effect Output signal consists of V-Sync and H-Sync information; There is one V-sync and 864 H-sync pulses per field:



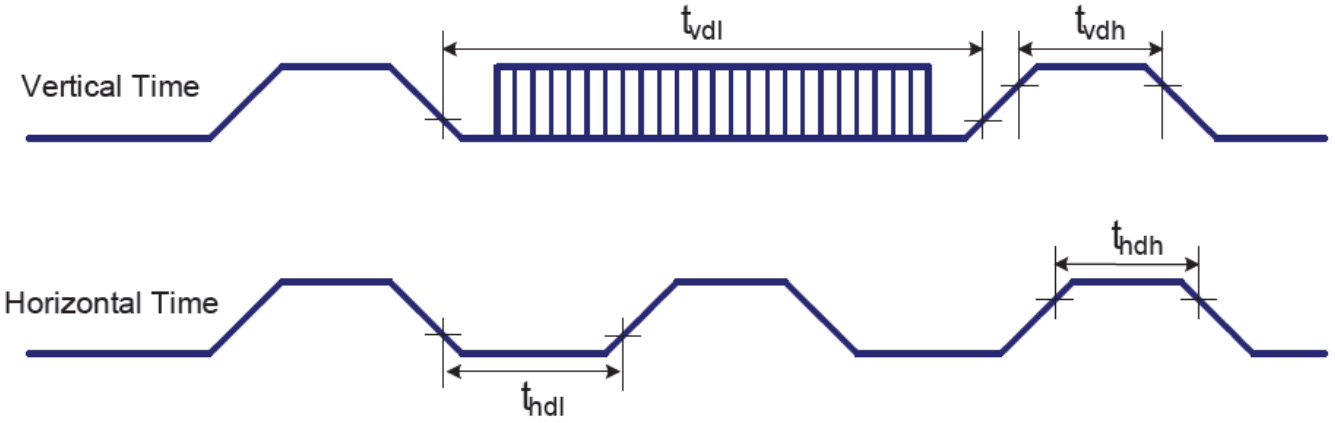
tvdh = The display panel is not updated from the Frame Memory.
tvdl = The display panel is updated from the Frame Memory (except Invisible Line – see below).
TE Line mode1 and Mode2 is shown as below graph:



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

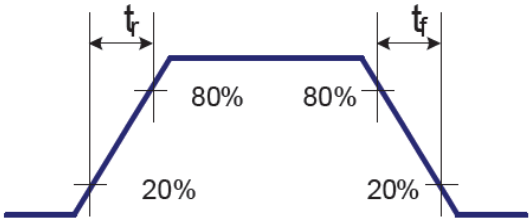
6.8.3 Tearing effect line timing

The Tearing Effect signal is described below:



Idle Mode Off/On

The TE signal rising and falling timing is described below:



6.9 Checksum

The display module consists of two 8-bit checksum registers, which are used to implement checksum calculations for area registers on the display module. One of the checksum registers is called “First Checksum” (FCS) and another one is called “Continue Checksum” (CCS). These registers will be set to 00h while a new checksum calculation starts.

Display module will start to calculate the new checksum after a write access on area registers, a set of registers which values can change a command register value directly. This means a read command will not trigger the calculation process in this case. The checksum calculation will always be interrupted when there is a new write access on area registers, and it will restart from the beginning. The result of the first checksum will be stored on the FCS register once after the calculation is finished. This value will be kept until there is a new write access on area registers. The maximum duration before the FCS can be read is 150ms after the last write access on area registers.

The checksum calculation will continue after the first checksum calculation finished, where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value will be replaced by a new one) after the last area register has been counted into the checksum. The maximum timing consumption, when the CCS is readable in the first time, is 300ms after the last write access on area registers.

The checksum comparison bit will always be updated after a new value is stored on CCS register. The maximum timing consumption, before the first comparison between FCS and CCS has been done, is 300ms, and then the comparison will be done every 150ms (the maximum value). Area can read FCS, CCS and Comparison bit D0 values. For further information, please refer to the command: “Read First Checksum (AAH)”, and “Read Continue Checksum (AFH)”.

Overflow might happeneded during a checksum calculation. These overflow bits are not necessarily

stored in anywhere, this means, it can be ignored by the display module.

An example of the checksum calculation:

- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function will only be executed during the “Sleep Out” mode and it will be stopped in “Sleep In” mode.

Checksum Sequence

Step Note 1	Time Note 2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on Nokia area registers => FCS and CCS registers are initialized.
2	0 – 150ms	Counting Sum of Nokia Area Registers	Counting	-	-	The first register counting is running
3	150ms	Stores Sum of Registers on FCS Register	Set to 00h after Value is Moved to FCS Register	Stores Sum of Nokia Area Registers on FCS Register	-	The result of the first register counting is stored on the FCS register. The result of the FCS is available to the MCU.
4	150 – 300ms	Counting Sum of Nokia Area Registers	Counting	-	-	The second register counting is running
5	300ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MCU.
6	300 – 450ms	Counting Sum of Nokia Area Registers	Counting	-	-	The third register counting is running
7	450ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU.
8	450 – 600ms	Counting Sum of Nokia Area Registers	Counting	-	-	The fourth register counting is running
9	600ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU.
10	etc	-	-	-	-	Same Sequence Countinue e.g. steps 4 and 5

Notes:

1. This function is restarted at Step 1 if there is any write action on area registers.
2. These time can be shorter on the display module.

6.10 OTP Programming Procedure

6.10.1 Powerfunction description

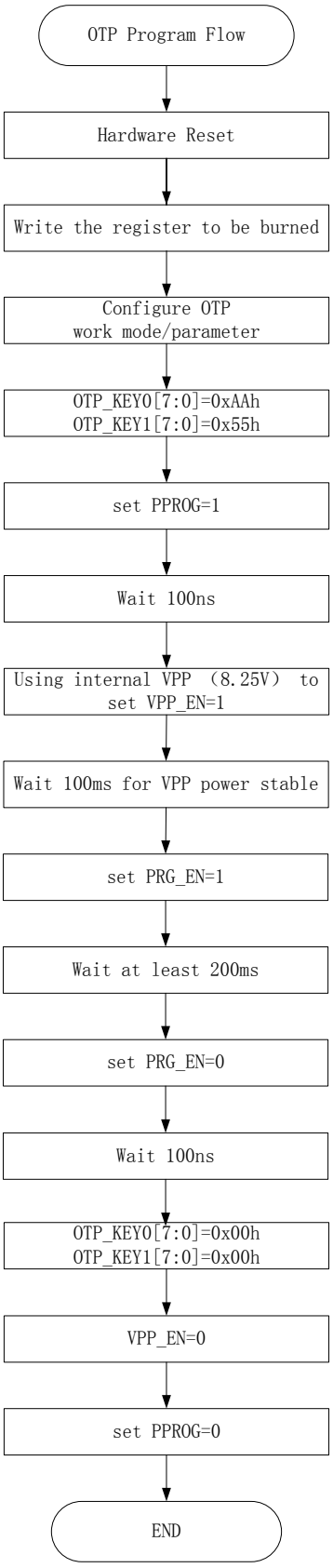
The OTP control signals control data reading and writing, only load once when reset. According to the request of the OTP, reset signal need delay at least 20ns to generate control signal. And signal transition should less than 1ns.

STEP: Write the register parameters, then using index read all index, if both consistent, to write read content into the OTP. This method requires each register readout parameters contend is same to written contend before. Each numbers of parameter is the same. And it may waste OTP resources if did not in byte. In order to prevent the wrong, the rest of resource as a reserve. The content behind can cover the front.

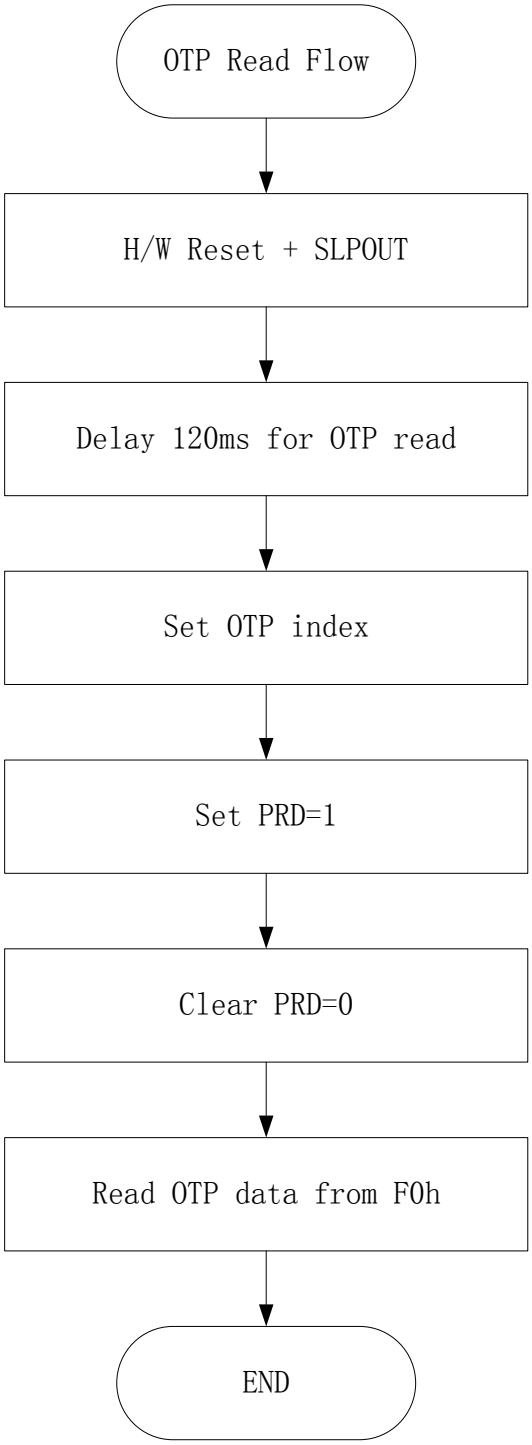
In program, Write the index and parameters, matching read contend with register number, and loading the content behind in register.

In addition, you can also loading OTP after reset release, and programming OTP by external interface generating timing.

6.10.2 OTP program flow chart


OTP Program Flow
Hardware Reset
Write the register to be burned
Configure OTP
work mode/parameter
OTP_KEY0[7:0]=0xAAh
OTP_KEY1[7:0]=0x55h
set PPROG=1
Wait 100ns
Using internal VPP (8.25V) to
set VPP_EN=1
Wait 100ms for VPP power stable
set PRG_EN=1
Wait at least 200ms
set PRG_EN=0
Wait 100ns
OTP_KEY0[7:0]=0x00h
OTP_KEY1[7:0]=0x00h
VPP_EN=0
set PPROG=0
END

6.10.3 OTP read program flow chart with External Power



When testing, connect signal with the test port, then observe the contend.

7 Electrical Specification

7.1 Absolute Maximum Ratings

(VDD=2.5V~6.0V, IOVCCO = 1.65V~3.6V, Ta = -30^{O}C ~ 70^{O}C)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	IOVCC-VSS	-0.3 ~ +4.5	V	
Power Supply Voltage 2	VSP-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 3	VSS-VSN	-0.3 ~ +6.6	V	
Power Supply Voltage 4	VDD-VSS	-0.3 ~ +1.5	V	
Power Supply Voltage 5	VPP-VSS	-0.3 ~ +9	V	
Power Supply Voltage 6	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ IOVCC+0.3	V	
Operating Temperature	Topr	-30 ~ +70	^{O}C	
Storage Temperature	Tstg	-40 ~ +85	^{O}C	

Note1:The maximum applicable voltage on any pin with respect to 0V.

Note2:Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

7.2 DC characteristic

7.2.1 Basic DC characteristic

(VSP=4.5V~6.5V, IOVCC = 1.65V~3.6V, Ta = -30^{o}C ~ 70^{o}C)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VSP	Operating Voltage	4.5	5.5	6.5	V	
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.6	V	
Digital Operating voltage	VDD	Digital supply voltage	-	1.5	-	V	
Input / Output							
Logic High level input voltage	V_{IH}	-	0.7 IOVCC	-	IOVCC	V	
Logic Low level input voltage	V_{IL}	-	VSS	-	0.3 IOVCC	V	
Logic High level output	V_{OH}	I_{OH} = -1.0mA	0.8	-	IOVCC	V	

voltage			IOVCC				
Logic Low level output voltage	V_{OL}	I_{OL} = +1.0mA	VSS	-	0.2 IOVCC	V	
Logic High level input current	I_{IH}	-	-	-	-	A	
Logic Low level input current	I_{IL}	-	-	-		A	
Logic Input leakage current	I_{IL}	VIN = IOVCC or VSS	-0.1	-	+0.1	A	
VCOM Operation							
VCOMDC voltage	VCOMDC	-	-4	-1.0	-0.3	V	Note1
Source Driver							
Source output range	Vsout	-	VSN+0.1	-	VSP-0.1	V	
Gamma positive reference voltage	VSPR	-	2.5	-	VSP-0.2	V	
Gamma negative reference voltage	VSNR	-	VSN+0.2	-	-2.5	V	
Source output settling time	Tr	Below with 99% precision	-	5	-	us	Note2
Output deviation voltage (Source positive output channel)	V,dev	Sout >=+4.2V, Sout<=+0.8V	-	-	30	mV	
		+4.2V>Sout>+0.8V	-	-	20	mV	
Output deviation voltage (Source negative output channel)	V,dev	Sout <=-4.2V, Sout>=-0.8V	-	-	30	mV	
		-4.2V<Sout<-0.8V	-	-	20	mV	
Output offset voltage	VOFSET	-	-	-	35	mV	
Reference Voltage							
Internal reference voltage	VREF		-	1.8	-	V	
Charge pump voltage							
VGH charge pump	VGH		10.0	15	16.3	V	
VGL charge pump	VGL		-13.3	-10	-7.0	V	
Current Consumption							
Sleep-IN mode(LP-11)	IVDDIO	RESX=High		TBD	TBD	uA	

(RAM power is ON)	IVDD			TBD	TBD	uA	
Sleep-IN mode(ULPS) (RAM power is OFF)	IVDDIO	RESX=High		TBD	TBD	uA	
	IVDD			TBD	TBD	uA	

Note1:The supported voltage range of VCOMDC depends on the applied VCL voltage.
Note2:The maximum applicable voltage on any pin with respect to 0V.

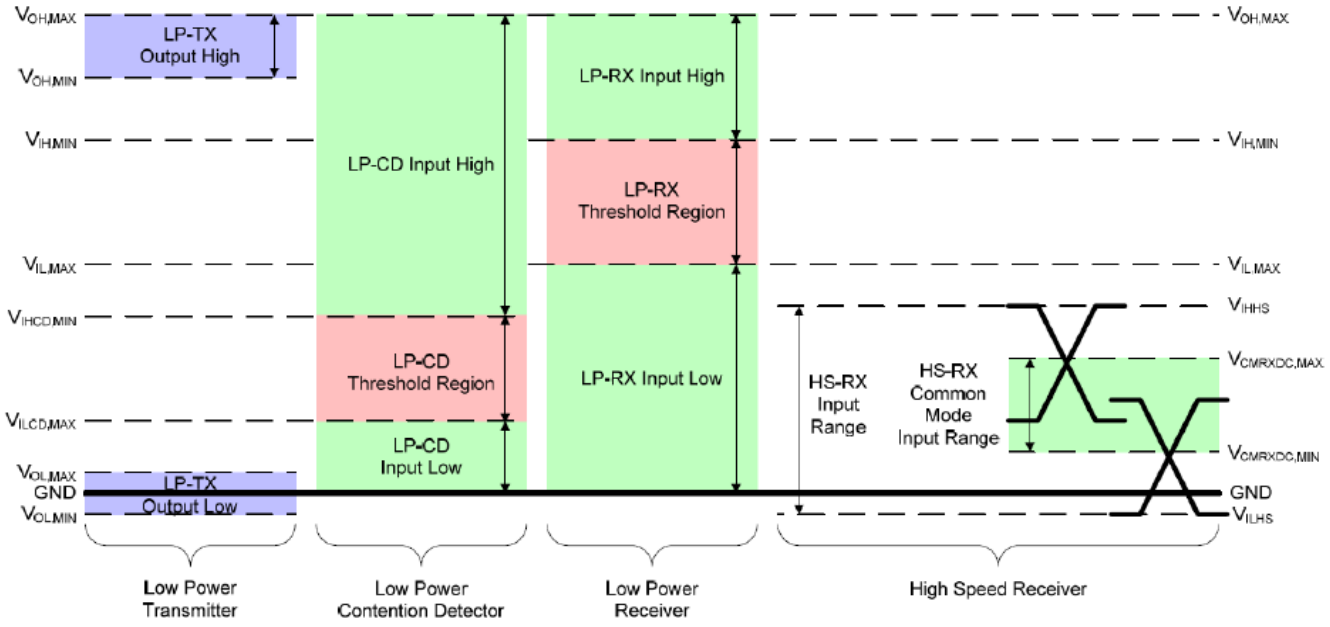
7.2.2 MIPI DC character

DC characteristics for MIPI-DSI

(VSP=4.5V~6.5V, IOVCC = 1.65V~3.6V, Ta = -30°C~ 70°C)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	HS_VDD	-	-	1.5	-	V
	HS_LDO	-	1.1	1.2	1.5	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	HS_VSS	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	HS_LDO	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.5	V
Logic 1 contention threshold	VIHCD,MIN	-	450	-	HS_LDO	mV
Logic 0 contention threshold	VILCD,MAX	-	0	-	200	mV
Output impedence of LPDT	ZOLP	-	80	-	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV

Differential input impedence	ZID	-	80	100	125	ohm



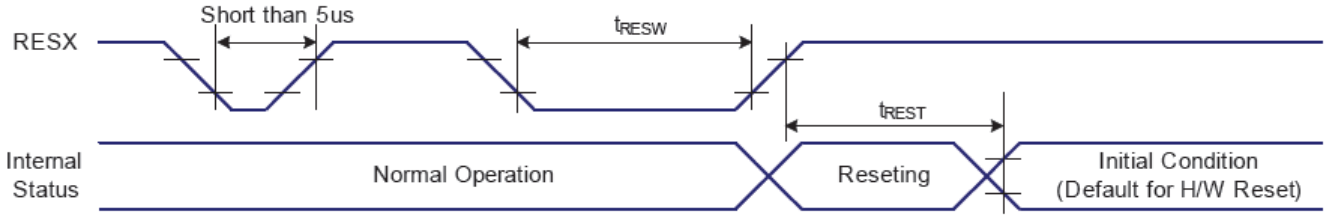
7.3 AC characteristic

7.3.1 TCON oscillator characteristics

Parameter	Symbol	Specification			Unit	Notes
		MIN	TYP	MAX		
Oscillator Frequency	Fosc0	-	37	-	MHz	
	Fosc1	-	38	-	MHz	
	Fosc2	-	39	-	MHz	
	Fosc3	-	40	-	MHz	
	Fosc4	-	41	-	MHz	
	Fosc5	-	42	-	MHz	
	Fosc6	-	43	-	MHz	
	Fosc7	-	44	-	MHz	
	Fosc8	-	45	-	MHz	
	Fosc9	-	46	-	MHz	
	Fosc10	-	47	-	MHz	
	Fosc11	-	48	-	MHz	
	Fosc12	-	49	-	MHz	

	Fosc13	-	50	-	MHz	
	Fosc14	-	51	-	MHz	
	Fosc15	-	52	-	MHz	

7.3.2 Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VSP=4.5V to 6.5V,Ta = -30°C to 70°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	**10**	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	**5**	When reset applied during Sleep in mode	ms
		-	-	-	**120**	When reset applied during Sleep out mode	ms

Table: Reset input timing

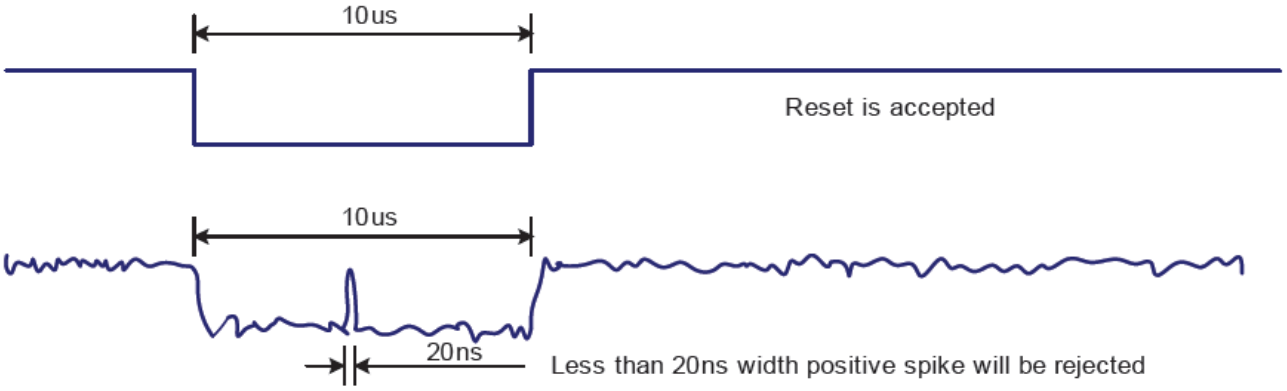
Note 1:Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2:During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3:During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4:Spike Rejection also applies during a valid reset pulse as shown below:



Note 5:It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

7.3.3 SPI interface characteristics

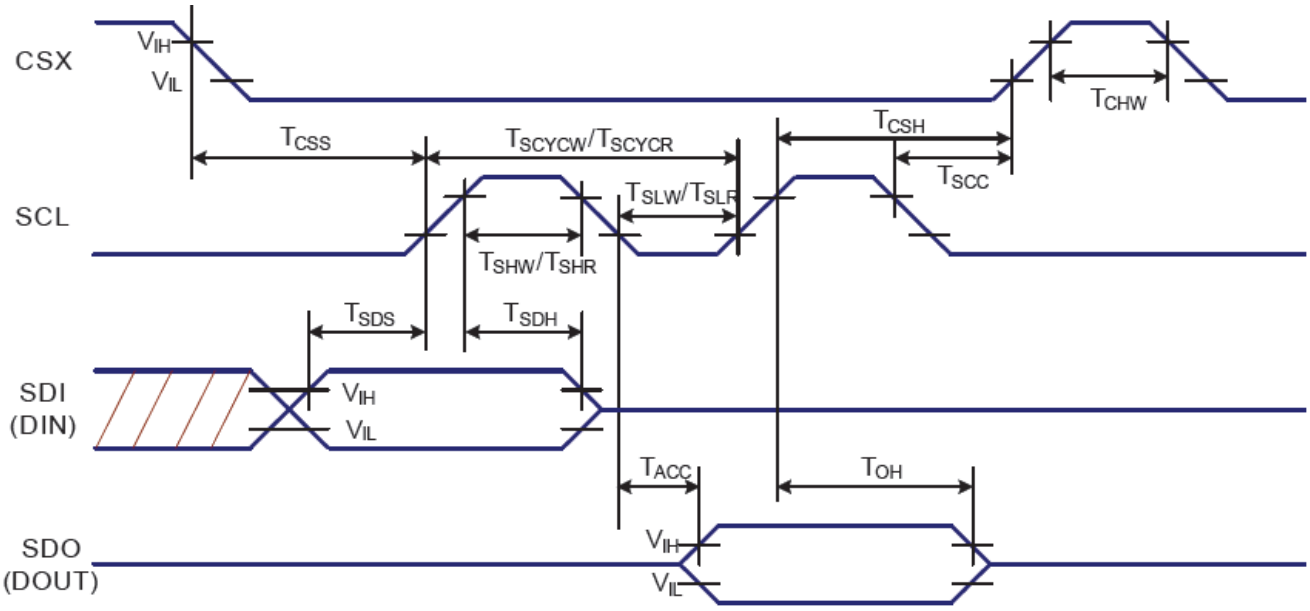


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

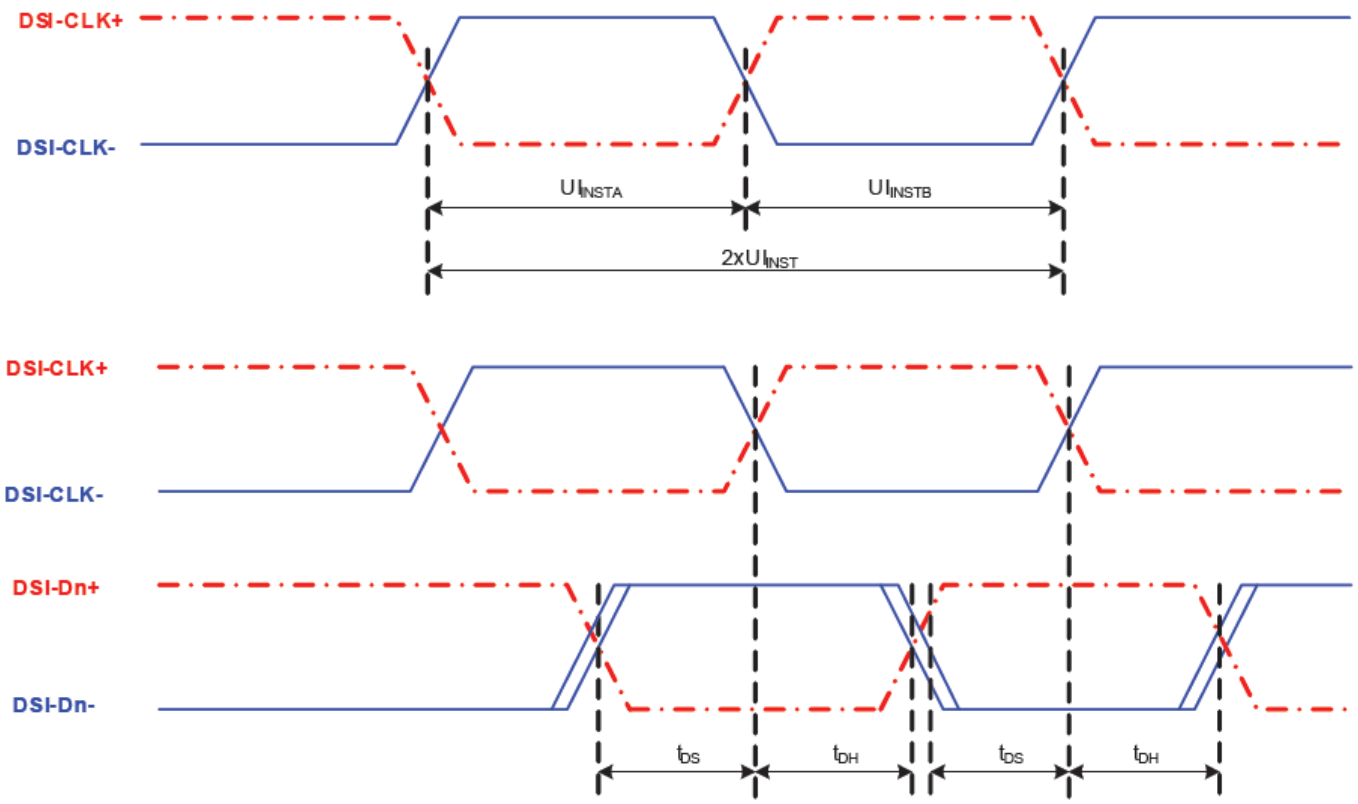
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	15	-	ns	-
	TCSH	Chip select hold time	15	-	ns	-
	TSCC	Chip select setup time	20	-	ns	-
	TCHW	Chip select setup time	40	-	ns	-
SCL	TSCYCW	Serial clock cycle (Write)	66	-	ns	-
	TSHW	SCL “H” pulse width (Write)	10	-	ns	-
	TSLW	SCL “L” pulse width (Write)	10	-	ns	-

	TSCYCR	Serial clock cycle (Read)	150	-	ns	-
	TSHR	SCL “H” pulse width (Read)	60	-	ns	-
	TSLR	SCL “L” pulse width (Read)	60	-	ns	-
SDA (DIN) (DOUT)	TSDS	Data setup time	10	-	ns	-
	TSDH	Data hold time	10	-	ns	-
	TACC	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	TOH	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VSP=4.5 to 6.5V, VSSA=VSS=0V, Ta= -30 to 70℃
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.3.4 MIPI-DSI characteristics

7.3.4.1 High speed mode



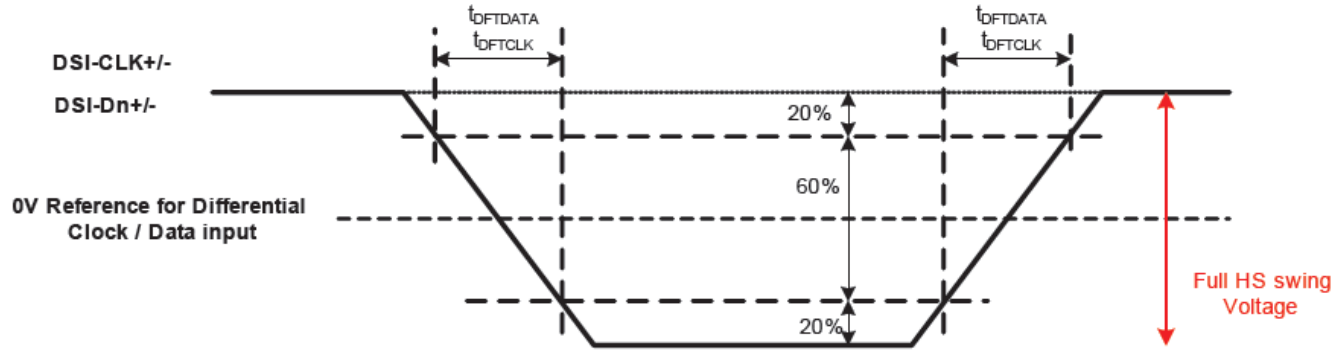


Figure: AC characteristics for MIPI-DSI High speed mode

7.3.4.2 Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP -11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP -11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T LPXD	-	2XT LPXD	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	5XT LPXD	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	4XT LPXD	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

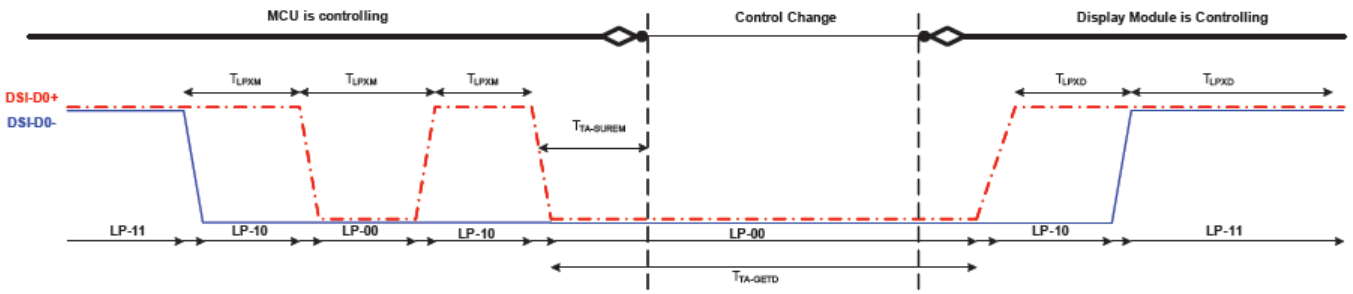


Figure: BTA from the MCU to the Display Module

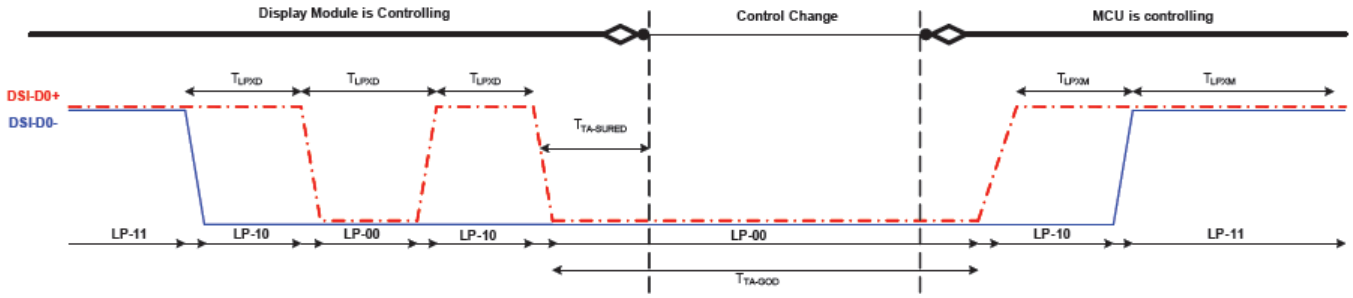


Figure: BTA from the Display Module to the MCU

7.3.4.3 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ Period to start of LP-11 state	-	-	105ns +12UI	ns

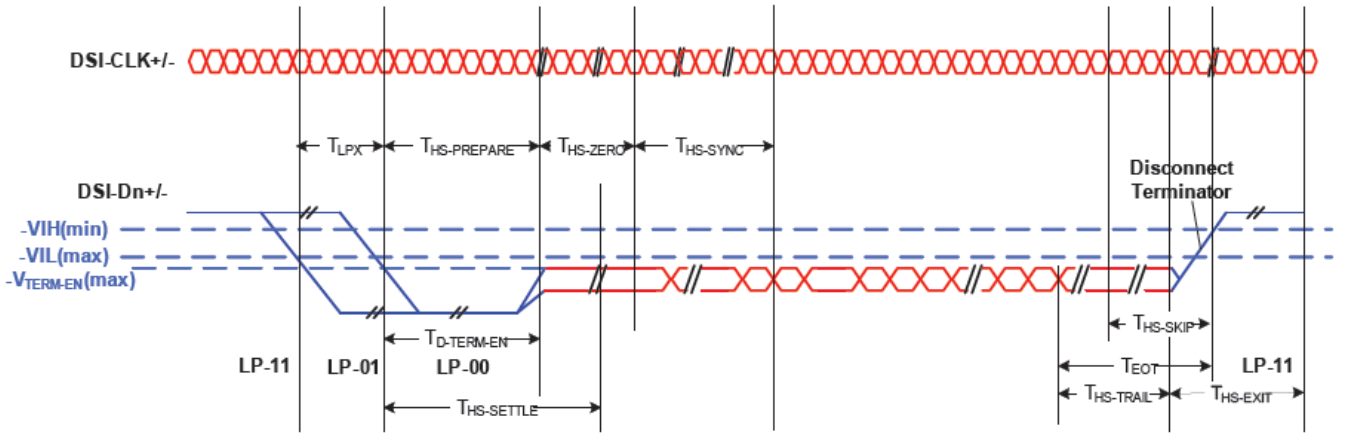


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lanehas transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lanebeginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$+ time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ periodto start of LP-11 state	-	-	105ns + 12UI	ns

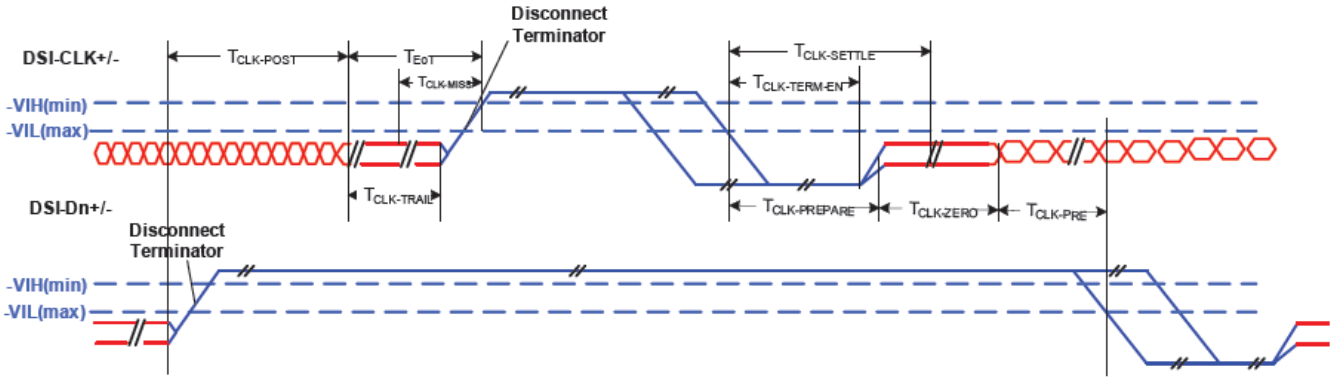


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

7.3.4.4 LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4

different combinations, what are listed below, are possible:

1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+52UI	-	60ns+52UI	-	60ns+52UI	-
BTA	100ns	-	100ns	-	100ns	-