1. Description

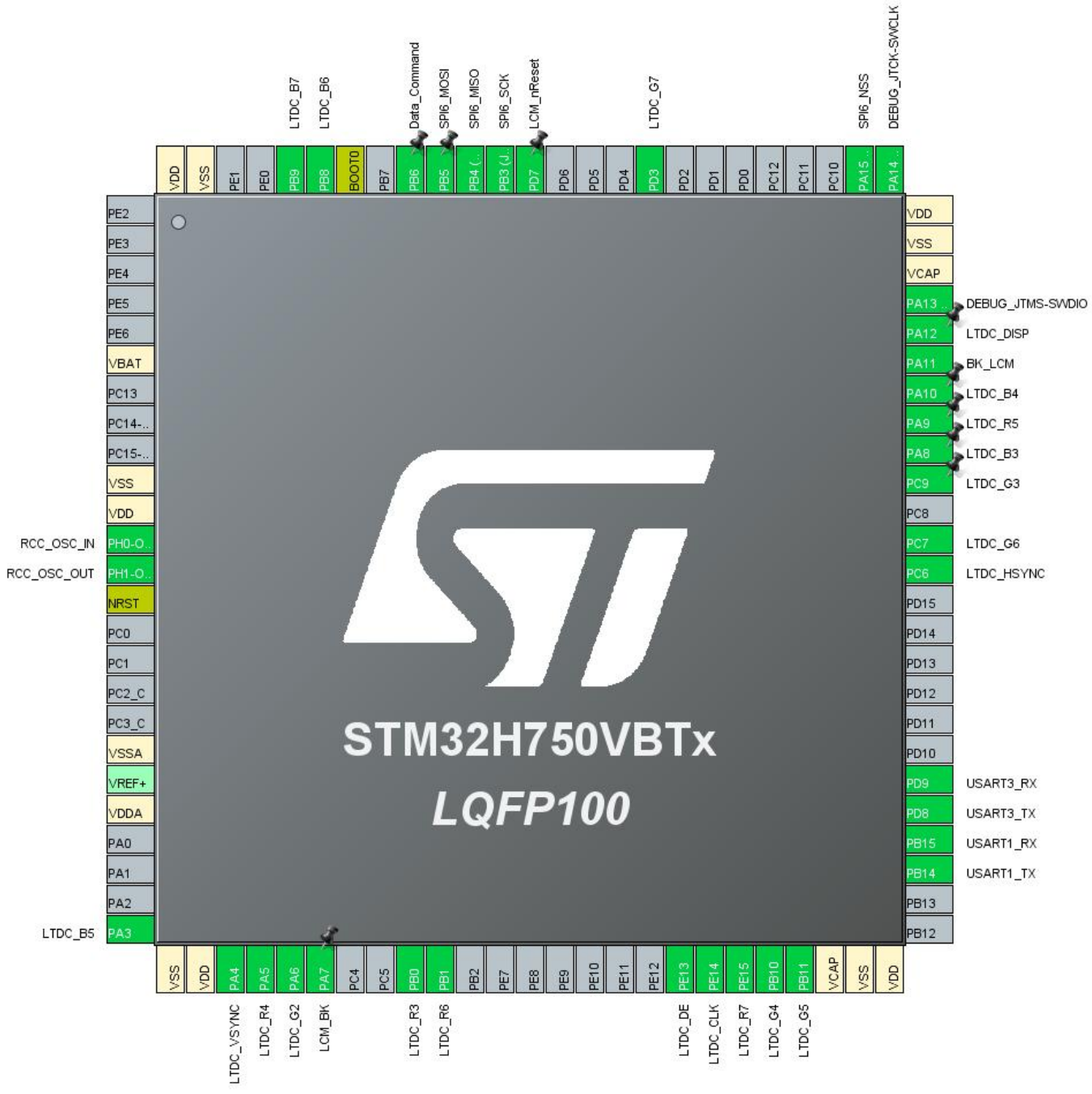
1.1. Project

Project Name	TFT_LCD_Demo_Board
Board Name	custom
Generated with:	STM32CubeMX 5.5.0
Date	02/13/2020

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H750 Value line
MCU name	STM32H750VBTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



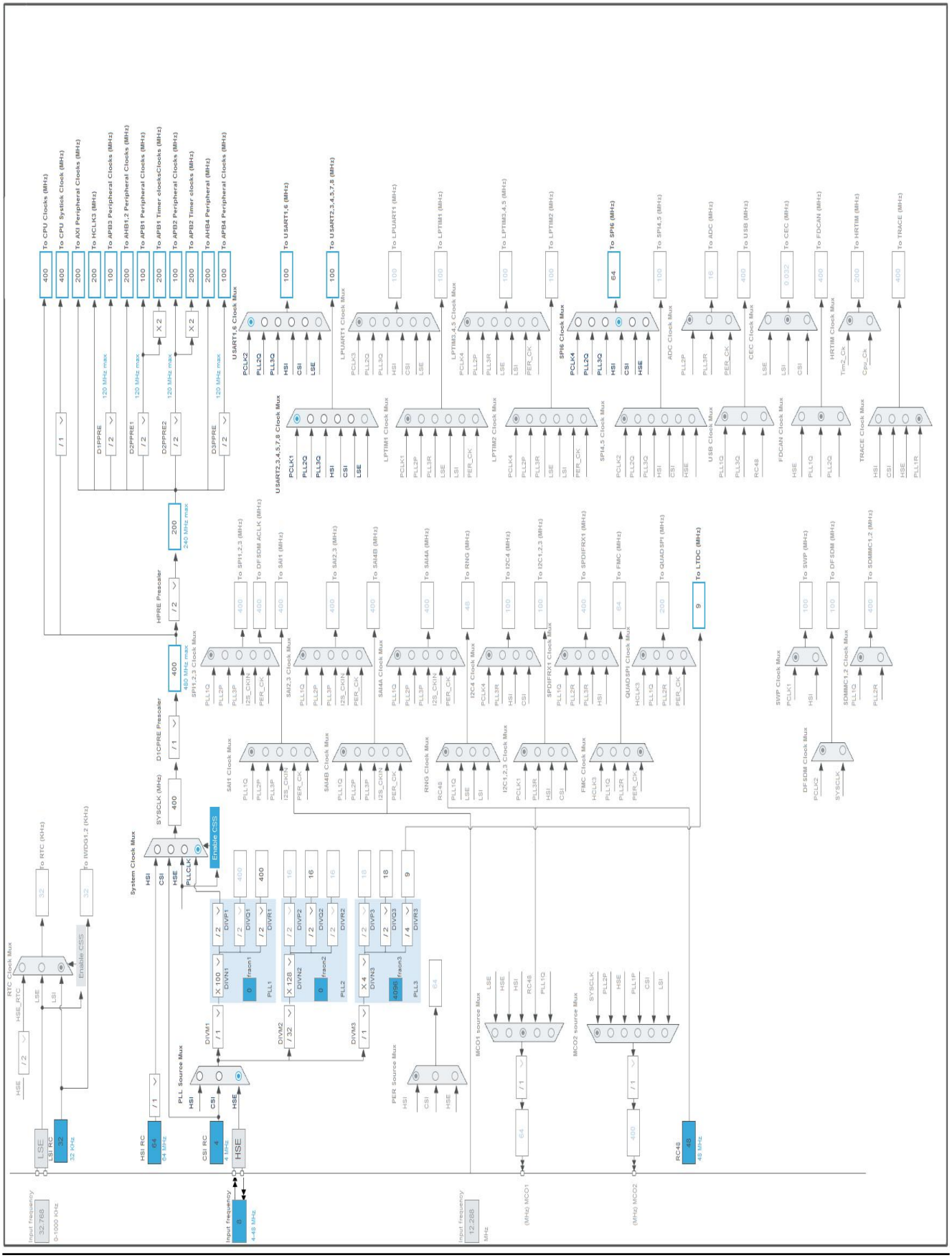
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VSSA	Power		
21	VDDA	Power		
25	PA3	I/O	LTDC_B5	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	LTDC_VSYNC	
29	PA5	I/O	LTDC_R4	
30	PA6	I/O	LTDC_G2	
31	PA7 *	I/O	GPIO_Output	LCM_BK
34	PB0	I/O	LTDC_R3	
35	PB1	I/O	LTDC_R6	
43	PE13	I/O	LTDC_DE	
44	PE14	I/O	LTDC_CLK	
45	PE15	I/O	LTDC_R7	
46	PB10	I/O	LTDC_G4	
47	PB11	I/O	LTDC_G5	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
53	PB14	I/O	USART1_TX	
54	PB15	I/O	USART1_RX	
55	PD8	I/O	USART3_TX	
56	PD9	I/O	USART3_RX	
63	PC6	I/O	LTDC_HSYNC	
64	PC7	I/O	LTDC_G6	
66	PC9	I/O	LTDC_G3	
67	PA8	I/O	LTDC_B3	
68	PA9	I/O	LTDC_R5	
69	PA10	I/O	LTDC_B4	
70	PA11	I/O	TIM1_CH4	BK_LCM

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
71	PA12 *	I/O	GPIO_Output	LTDC_DISP
72	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
77	PA15 (JTDI)	I/O	SPI6_NSS	
84	PD3	I/O	LTDC_G7	
88	PD7 *	I/O	GPIO_Output	LCM_nReset
89	PB3 (JTDO/TRACESWO)	I/O	SPI6_SCK	
90	PB4 (NJTRST)	I/O	SPI6_MISO	
91	PB5	I/O	SPI6_MOSI	
92	PB6 *	I/O	GPIO_Output	Data_Command
94	BOOT0	Boot		
95	PB8	I/O	LTDC_B6	
96	PB9	I/O	LTDC_B7	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	TFT_LCD_Demo_Board
Project Folder	D:\STM32CubeMX\STM32H750VBT6\Test\TFT_LCD_Demo_Board
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_H7 V1.6.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H750 Value line
MCU	STM32H750VBTx
Datasheet	DS12556_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.2. DEBUG

Debug: Serial Wire

7.3. GPIO

7.4. LTDC

Display Type: RGB565 (16 bits)

7.4.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**41 ***
Horizontal Back Porch	**2 ***
Active Width	**480 ***
Horizontal Front Porch	**2 ***
HSync Width	40
Accumulated Horizontal Back Porch Width	42
Accumulated Active Width	522
Total Width	524

Synchronization for Height:

Vertical Synchronization Height	**10 ***
Vertical Back Porch	2
Active Height	**272 ***
Vertical Front Porch	2
VSync Height	9
Accumulated Vertical Back Porch Height	11
Accumulated Active Height	283

Total Height	285

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	**255 ***
Green	**255 ***
Blue	**255 ***

7.4.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**480 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**272 ***

Pixel Parameters:

Layer 0 - Pixel Format	**RGB565 ***

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	**480 ***
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**272 ***

Number of Layers:

Number of Layers	**1 layer ***

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL3 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL3 clock Output range	Wide VCO range

7.6. SPI6

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Input Signal

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***
Baud Rate	**1000.0 KBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Input Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.7. SYS

Timebase Source: SysTick

7.8. TIM1

Channel4: PWM Generation CH4

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable

- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.9. TIM14

mode: Activated

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

7.10. USART1

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.11. USART3

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. FREERTOS

Interface: CMSIS_V1

7.12.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8

USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.12.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled

vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
LTDC	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA5	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PE13	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PE14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC9	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA8	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA9	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA10	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI6	PA15 (JTDI)	SPI6_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3 (JTDO/TRACESWO)	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM1	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	BK_LCM
USART1	PB14	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PA7	GPIO_Output	Output Push Pull	**Pull-up ***	Low	LCM_BK
	PA12	GPIO_Output	Output Push Pull	**Pull-up ***	Low	LTDC_DISP
	PD7	GPIO_Output	Output Push Pull	**Pull-up ***	Low	LCM_nReset
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Data_Command

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Stream0	Peripheral To Memory	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low

USART1_RX: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
LTDC global interrupt	true	5	0
LTDC global error interrupt	true	5	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
USART1 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
FPU global interrupt	unused		
SPI6 global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

9. Software Pack Report

9.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	FreeRTOS	0.0.1	Class : CMSIS Group : RTOS SubGroup : FreeRTOS Version : 10.2.0 Class : RTOS Group : Core Version : 10.2.0