

Im Using STM32F767ZI Nucleo Board which has 2Mbytes of flash for code storage. It also allows for the flash to be evenly divided between two banks. This gives bank 1 one Mbyte of data, and bank 2 one Mbyte of data.

Bank 1 Address offset in Flash is 0x08000000

Bank 2 Address offset in Flash is 0x08100000

With the use of nDBOOT = nDBANK = 0 option bytes the memory is configured in the dual bank, dual boot mode.

My Current Testing Procedure:

Step 1) I compile the firmware which has a single byte indicating the version of the firmware. I compile it twice once with version byte as 1, and once with version byte as 2. Otherwise its identical code.

Step 2) I use STM32 ST-Link Utility to manually program each version into each bank and run it. I do this for both version with both banks, so 4 times.

I use the following option bytes to run from bank 1 while programming the .bin at offset for Bank 1:

Option Bytes ×

Read Out Protection
Level 0

BOR Level
F Level 0 R

User configuration option byte

<input type="checkbox"/> IWDG_STOP	<input type="checkbox"/> IWDG_STDBY	<input type="checkbox"/> nBoot0	<input type="checkbox"/> nBOOT0
<input checked="" type="checkbox"/> WWDG_SW	<input type="checkbox"/> IWDG_ULP	<input type="checkbox"/> nBoot1	<input type="checkbox"/> BOOT1
<input type="checkbox"/> nSRAM_Parity	<input checked="" type="checkbox"/> FZ_IWDG_STOP	<input type="checkbox"/> nDBOOT	<input type="checkbox"/> nBFB2
<input type="checkbox"/> SRAM2_RST	<input checked="" type="checkbox"/> FZ_IWDG_STDBY	<input type="checkbox"/> nDBANK	<input type="checkbox"/> nBOOT_SEL
<input type="checkbox"/> SRAM2_PE	<input type="checkbox"/> PCROP_RDP	<input type="checkbox"/> DB1M	<input type="checkbox"/> DUALBANK
<input type="checkbox"/> nRST_SHDW	<input type="checkbox"/> nBoot0_SW_Cfg	<input type="checkbox"/> IRHEN	<input type="checkbox"/> BOREN
<input checked="" type="checkbox"/> nRST_STOP	<input type="checkbox"/> nSWBOOT0	<input checked="" type="checkbox"/> IWDG_SW	
<input checked="" type="checkbox"/> nRST_STDBY	<input type="checkbox"/> VDDA_Monitor	<input type="checkbox"/> SDADC12_VDD_Monitor	

NRST_MODE

Security option bytes

SEC_SIZE 0x00 ☐ BOOT_LOCK

Boot address option bytes

BOOT_ADD0 (H) 0x2000	Boot from (H) 0x08000000
BOOT_ADD1 (H) 0x2040	Boot from (H) 0x08100000

Once its all done i use the following code to actually switch the banks

So for Step 3 This works. It loads version 2 into Bank 2 and starts running it. I can see version 2 being output, and after i hit hard reset it again loads the new firmware from Bank 2. All is as expected here.

When i try to program version 1 or version 2 into Bank 2 and run the upgrade process it never is able to program anything into bank 1. It can erase it but the actual program never happens even though no errors are reported except when it actually tries to verify the memory against the live data. When i look at the Bank 1 memory after programming from Bank 2 its all 0xFFFF.

-Andriy