1. STUSB_1_3 Component

1. STUSB_1_3

Vendor	Library	Name	Version
st.com	Leon2	STUSB	1.3

2. SPIRIT address block STUSB_MAP

Base address	Size	Address block	Description
0x0	0x1000	STUSB_BLOCK	

STUSB_BLOCK Register Summary

3. STUSB_BLOCK register list

Offset	Register name	Description	Page
0x06	BCD_TYPEC_REV_LOW	BCD_TYPEC_REV_LOW register	0
0x07	BCD_TYPEC_REV_HIGH	BCD_TYPEC_REV_HIGH register	0
0x08	BCD_USBPD_REV_LOW	BCD_USBPD_REV_LOW register	0
0x09	BCD_USBPD_REV_HIGH	BCD_USBPD_REV_HIGH register	0
0x0A	DEVICE_CAPAB_HIGH	DEVICE_CAPAB_HIGH register	0
0x0B	ALERT_STATUS_1	ALERT_STATUS_1 register	0
0x0C	ALERT_STATUS_1_MASK	ALERT_STATUS_1_MASK register	0
0x0D	PORT_STATUS_0	PORT_STATUS_0 register	0
0x0E	PORT_STATUS_1	PORT_STATUS_1 register	0
0x0F	TYPEC_MONITORING_STATUS_0	TYPEC_MONITORING_STATUS_0 register	0
0x10	TYPEC_MONITORING_STATUS_1	TYPEC_MONITORING_STATUS_1 register	0
0x11	CC_STATUS	CC_STATUS register	0
0x12	CC_HW_FAULT_STATUS_0	CC_HW_FAULT_STATUS_0 register	0
0x13	CC_HW_FAULT_STATUS_1	CC_HW_FAULT_STATUS_1 register	0
0x16	PRT_STATUS	PRT_STATUS register	0
0x17	PHY_STATUS	PHY_STATUS register	0
0x18	reserved	reserved	
0x19	reserved	reserved	
0x1A	PD_COMMAND	PD_COMMAND register	0
0x1B	reserved	reserved	
0x1D	DEVICE_CTRL	DEVICE_CTRL register	0
0x1E	ANALOG_CNTRL	ANALOG_CNTRL register	0
0x1F	reserved	reserved	
0x20	MONITORING_CTRL_0	MONITORING_CTRL_0 register	0
0x21	MONITORING_CTRL_1	MONITORING_CTRL_1 register	0
0x22	MONITORING_CTRL_2	MONITORING_CTRL_2 register	0
0x23	RESET_CTRL	RESET_CTRL register	RESET_CTRL
0x24	POWER_ACCESSORY_CTRL	POWER_ACCESSORY_CTRL register	POWER_ACCESSORY_CTRL

0x25	VBUS_DISCHARGE_TIME_CTRL	VBUS_DISCHARGE_TIME_CTRL register	VBUS_0
0x26	VBUS_DISCHARGE_CTRL	VBUS_DISCHARGE_CTRL register	VBUS_0
0x27	VBUS_CTRL	VBUS_CTRL register	0
0x28	POWER_ROLE_CTRL	POWER_ROLE_CTRL register	POWER_ROLE_CTRL
0x29	PE_FSM	PE_FSM register	**Error! Reference source not found.**
0x2E	SPARE_BITS	SPARE_BITS register	0
0x2F	DEVICE_ID	DEVICE_ID register	0
0x30	reserved	reserved	
0x31	RX_HEADER_LOW	RX_HEADER_LOW register	0
0x32	RX_HEADER_HIGH	RX_HEADER_HIGH register	0
0x33	RX_DATA_OBJ1_0	RX_DATA_OBJ1_0 register	0
0x34	RX_DATA_OBJ1_1	RX_DATA_OBJ1_1 register	
0x35	RX_DATA_OBJ1_2	RX_DATA_OBJ1_2 register	
0x36	RX_DATA_OBJ1_3	RX_DATA_OBJ1_3 register	
0x37	RX_DATA_OBJ2_0	RX_DATA_OBJ2_0 register	0
0x38	RX_DATA_OBJ2_1	RX_DATA_OBJ2_1 register	
0x39	RX_DATA_OBJ2_2	RX_DATA_OBJ2_2 register	
0x3A	RX_DATA_OBJ2_3	RX_DATA_OBJ2_3 register	
0x3B	RX_DATA_OBJ3_0	RX_DATA_OBJ3_0 register	0
0x3C	RX_DATA_OBJ3_1	RX_DATA_OBJ3_1 register	
0x3D	RX_DATA_OBJ3_2	RX_DATA_OBJ3_2 register	
0x3E	RX_DATA_OBJ3_3	RX_DATA_OBJ3_3 register	
0x3F	RX_DATA_OBJ4_0	RX_DATA_OBJ4_0 register	0
0x40	RX_DATA_OBJ4_1	RX_DATA_OBJ4_1 register	
0x41	RX_DATA_OBJ4_2	RX_DATA_OBJ4_2 register	
0x42	RX_DATA_OBJ4_3	RX_DATA_OBJ4_3 register	
0x43	RX_DATA_OBJ5_0	RX_DATA_OBJ5_0 register	0
0x44	RX_DATA_OBJ5_1	RX_DATA_OBJ5_1 register	
0x45	RX_DATA_OBJ5_2	RX_DATA_OBJ5_2 register	
0x46	RX_DATA_OBJ5_3	RX_DATA_OBJ5_3 register	
0x47	RX_DATA_OBJ6_0	RX_DATA_OBJ6_0 register	0
0x48	RX_DATA_OBJ6_1	RX_DATA_OBJ6_1 register	
0x49	RX_DATA_OBJ6_2	RX_DATA_OBJ6_2 register	
0x4A	RX_DATA_OBJ6_3	RX_DATA_OBJ6_3 register	
0x4B	RX_DATA_OBJ7_0	RX_DATA_OBJ7_0 register	0
0x4C	RX_DATA_OBJ7_1	RX_DATA_OBJ7_1 register	
0x4D	RX_DATA_OBJ7_2	RX_DATA_OBJ7_2 register	
0x4E	RX_DATA_OBJ7_3	RX_DATA_OBJ7_3 register	
0x50 0x6F	reserved	reserved	
0x70	DPM_PDO_NUMB	DPM_PDO_NUMB register	0
0x71	DPM_SRC_PDO1_0	DPM_SRC_PDO1_0 register	0
0x72	DPM_SRC_PDO1_1	DPM_SRC_PDO1_1 register	
0x73	DPM_SRC_PDO1_2	DPM_SRC_PDO1_2 register	
0x74	DPM_SRC_PDO1_3	DPM_SRC_PDO1_3 register	

0x75	DPM_SRC_PDO2_0	DPM_SRC_PDO2_0 register	
0x76	DPM_SRC_PDO2_1	DPM_SRC_PDO2_1 register	
0x77	DPM_SRC_PDO2_2	DPM_SRC_PDO2_2 register	
0x78	DPM_SRC_PDO2_3	DPM_SRC_PDO2_3 register	
0x79	DPM_SRC_PDO3_0	DPM_SRC_PDO3_0 register	
0x7A	DPM_SRC_PDO3_1	DPM_SRC_PDO3_1 register	
0x7B	DPM_SRC_PDO3_2	DPM_SRC_PDO3_2 register	
0x7C	DPM_SRC_PDO3_3	DPM_SRC_PDO3_3 register	
0x7D	DPM_SRC_PDO4_0	DPM_SRC_PDO4_0 register	
0x7E	DPM_SRC_PDO4_1	DPM_SRC_PDO4_1 register	
0x7F	DPM_SRC_PDO4_2	DPM_SRC_PDO4_2 register	
0x80	DPM_SRC_PDO4_3	DPM_SRC_PDO4_3 register	
0x81	DPM_SRC_PDO5_0	DPM_SRC_PDO5_0 register	
0x82	DPM_SRC_PDO5_1	DPM_SRC_PDO5_1 register	
0x83	DPM_SRC_PDO5_2	DPM_SRC_PDO5_2 register	
0x84	DPM_SRC_PDO5_3	DPM_SRC_PDO5_3 register	
0x85 0x90	reserved	reserved	
0x91	DPM_REQ_RDO3_0	DPM_REQ_RDO3_0 register	**Error! Reference source not found.**
0x92	DPM_REQ_RDO3_1	DPM_REQ_RDO3_1 register	
0x93	DPM_REQ_RDO3_2	DPM_REQ_RDO3_2 register	
0x94	DPM_REQ_RDO3_3	DPM_REQ_RDO3_3 register	

STUSB_BLOCK register descriptions

BCD_TYPEC_REV_LOW

BCD_TYPEC_REV_LOW register

7	6	5	4	3	2	1	0
BCD_TYPEC_REV_7_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x06

Type: R

Reset: 0x12

Description: BCD_TYPEC_REV_LOW register

[7:0]	**BCD_TYPEC_REV_7_0**: Defined Type-C release supported by the device

BCD_TYPEC_REV_HIGH

BCD_TYPEC_REV_HIGH register

7	6	5	4	3	2	1	0
BCD_TYPEC_REV_15_8							
R							

Address: STUSB_BLOCKBaseAddress + 0x07

Type: R

Reset: 0x00

Description: BCD_TYPEC_REV_HIGH register

[7:0]	**BCD_TYPEC_REV_15_8**: Defined Type-C release supported by the device

BCD_USBPD_REV_LOW

BCD_USBPD_REV_LOW register

7	6	5	4	3	2	1	0
BCD_USBPD_REV_7_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x08

Type: R

Reset: 0x11

Description: BCD_USBPD_REV_LOW register

[7:0]	**BCD_USBPD_REV_7_0**: Defined Power Delivery release supported by the device

BCD_USBPD_REV_HIGH

BCD_USBPD_REV_HIGH register

7	6	5	4	3	2	1	0
BCD_USBPD_REV_15_8							
R							

Address: STUSB_BLOCKBaseAddress + 0x09

Type: R

Reset: 0x20

Description: BCD_USBPD_REV_HIGH register

[7:0]	**BCD_USBPD_REV_15_8**: Defined Power Delivery release supported by the device

DEVICE_CAPAB_HIGH

DEVICE_CAPAB_HIGH register

7	6	5	4	3	2	1	0
DEVICE_CAPAB_HIGH							
R							

Address: STUSB_BLOCKBaseAddress + 0x0A

Type: R

Reset: 0x00

Description: DEVICE_CAPAB_HIGH register

[7:0]	**DEVICE_CAPAB_HIGH**: Not used

ALERT_STATUS_1

ALERT_STATUS_1 register

7	6	5	4	3	2	1	0
HARD_RESET_AL	PORT_STATUS_AL	TYPEC_MONITORING_STATUS_AL	CC_HW_FAULT_STATUS_AL	RESERVED	RESERVED	PRT_STATUS_AL	PHY_STATUS_AL
RC	R	R	R	R	R	R	R

Address: STUSB_BLOCKBaseAddress + 0x0B

Type: R

Reset: 0x30

Description: ALERT_STATUS_1 register

[7]	**HARD_RESET_AL**: TBD
[6]	**PORT_STATUS_AL**: TBD
[5]	**TYPEC_MONITORING_STATUS_AL**: TBD
[4]	**CC_HW_FAULT_STATUS_AL**: TBD
[1]	**PRT_STATUS_AL**: TBD
[0]	**PHY_STATUS_AL**: TBD

ALERT_STATUS_1_MASK

ALERT_STATUS_1_MASK register

7	6	5	4	3	2	1	0
HARD_RESET_AL_MASK	PORT_STATUS_AL_MASK	TYPEC_MONITORING_STATUS_MASK	CC_FAULT_STATUS_AL_MASK	RESERVED	RESERVED	PRT_STATUS_AL_MASK	PHY_STATUS_AL_MASK
R/W	R/W	R/W	R/W	R	R	R/W	R/W

Address: STUSB_BLOCKBaseAddress + 0x0C

Type: R/W

Reset: 0xFF

Description: ALERT_STATUS_1_MASK register

[7]	**HARD_RESET_AL_MASK** 0: (UNMASKED) Interrupt unmasked 1: (MASKED) Interrupt masked Initiated by FTP_ALERT_STATUS_1_MASK[7]
[6]	**PORT_STATUS_AL_MASK** 0: (UNMASKED) Interrupt unmasked 1: (MASKED) Interrupt masked Initiated by FTP_ALERT_STATUS_1_MASK[6]
[5]	**TYPEC_MONITORING_STATUS_MASK** 0: (UNMASKED) Interrupt unmasked 1: (MASKED) Interrupt masked Initiated by FTP_ALERT_STATUS_1_MASK[5]
[4]	**CC_FAULT_STATUS_AL_MASK** 0: (UNMASKED) Interrupt unmasked 1: (MASKED) Interrupt masked Initiated by FTP_ALERT_STATUS_1_MASK[4]
[1]	**PRT_STATUS_AL_MASK**: 0: (UNMASKED) Interrupt unmasked 1: (MASKED) Interrupt masked Initiated by FTP_ALERT_STATUS_1_MASK[1]
[0]	**PHY_STATUS_AL_MASK**: 0: (UNMASKED) Interrupt unmasked 1: (MASKED) Interrupt masked Initiated by FTP_ALERT_STATUS_1_MASK[0]

PORT_STATUS_0

PORT_STATUS_0 register

7	6	5	4	3	2	1	0
RESERVED							ATTACH_TRANS
R							RC

Address: STUSB_BLOCKBaseAddress + 0x0D

Type: R

Reset: 0x00

Description: PORT_STATUS_0 register

[0]	**ATTACH_TRANS**: 1: Transition detected in Attached state

PORT_STATUS_1

PORT_STATUS_1 register

7	6	5	4	3	2	1	0
ATTACHED_DEVICE			LOW_POWER_STANDBY	POWER_MODE	DATA_MODE	VCONN_MODE	ATTACH
R			R	R	R	R	R

Address: STUSB_BLOCKBaseAddress + 0x0E

Type: RC

Reset: 0x00

Description: PORT_STATUS_1 register

[7:5]	**ATTACHED_DEVICE**: 000: (NONE_ATT) No device connected 001: (SNK_ATT) Sink device connected 010: (SRC_ATT) Source device connected 011: (DBG_ATT) Debug accessory device connected 100: (AUD_ATT) Audio accessory device connected 101: (POW_ACC_ATT) Powered accessory device connected Others: Do not use
[4]	**LOW_POWER_STANDBY**: 0: (LP_OFF) Device is operating in normal mode 1: (LP_ON) Device is operating in standby mode
[3]	**POWER_MODE**: 0: (POW_SNK) 1: (POW_SRC)
[2]	**DATA_MODE**: 0: (UFP) 1: (DFP)
[1]	**VCONN_MODE**: 0: (VCONN_OFF) VCONN is not supplied 1: (VCONN_ON) VCONN is supplied
[0]	**ATTACH**: 0: (UNATTACHED) 1: (ATTACHED)

TYPEC_MONITORING_STATUS_0

TYPEC_MONITORING_STATUS_0 register

7	6	5	4	3	2	1	0
PD_TYPEC_HAND_CHECK				VBUS_READY_TRANS	VBUS_VSAFE0V_TRANS	VBUS_VALID_TRANS	VCONN_VALID_TRANS
RC				RC	RC	RC	RC

Address: STUSB_BLOCKBaseAddress + 0x0F

Type: R

Reset: 0x0F

Description: TYPEC_MONITORING_STATUS_0 register

[7:4]	**PD_TYPEC_HAND_CHECK**: hand checking sent by Type C to Power Delivery to feedback requested action 0000:cleared 0001:PD_PR_SWAP_PS_RDY_ACK 0010:PD_PR_SWAP_RP_ASSERT_ACK 0011:PD_PR_SWAP_RD_ASSERT_ACK 0100:PD_DR_SWAP_PORT_CHANGE_2_DFP_ACK 0101:PD_DR_SWAP_PORT_CHANGE_2_UFP_ACK 0110:PD_VCONN_SWAP_TURN_ON_VCONN_ACK 0111:PD_VCONN_SWAP_TURN_OFF_VCONN_ACK 1000:PD_HARD_RESET_COMPLETE_ACK 1001:PD_HARD_RESET_TURN_OFF_VCONN_ACK 1010:PD_HARD_RESET_PORT_CHANGE_2_DFP_ACK 1011:PD_HARD_RESET_PORT_CHANGE_2_UFP_ACK 1100:PD_PR_SWAP_SNK_VBUS_OFF_ACK 1101:PD_PR_SWAP_SRC_VBUS_OFF_ACK 1110:PD_HARD_RESET_RECEIVED_ACK 1111:PD_HARD_RESET_SEND_ACK
[3]	**VBUS_READY_TRANS**: 0: status cleared 1: Transition detected on VBUS_READY bit
[2]	**VBUS_VSAFE0V_TRANS**: 0: status cleared 1: Transition detected on VBUS_VSAFE0V bit
[1]	**VBUS_VALID_TRANS**: 0: status cleared 1: Transition detected on VBUS_VALID bit
[0]	**VCONN_VALID_TRANS**: 0: (NO_TRANS) Status cleared 1: (TRANS_DETECTED) Transition detected on VCONN_VALID bit

TYPEC_MONITORING_STATUS_1

TYPEC_MONITORING_STATUS_1 register

7	6	5	4	3	2	1	0
RESERVED				VBUS_READY	VBUS_VSAFE0V	VBUS_VALID	VCONN_VALID
R				R	R	R	R

Address: STUSB_BLOCKBaseAddress + 0x10

Type: R

Reset: 0x0E

Description: TYPEC_MONITORING_STATUS_1 register

[3]	**VBUS_READY**: 0: VBUS disconnected (Unpowered or vSafe0V) 1: VBUS connected (vSafe5V or negotiated power level)
[2]	**VBUS_VSAFE0V**: 0: VBUS is higher than 0.8V 1: VBUS is lower than 0.8V
[1]	**VBUS_VALID**: 0: VBUS is lower than 3.9V 1: VBUS is higher than 3.9V
[0]	**VCONN_VALID**: 0: VCONN is lower than 4.1V or 2.7V 1: VCONN is higher than 4.1V or 2.7V

CC_STATUS

CC_STATUS register

7	6	5	4	3	2	1	0
REVERSE	SNK_POWER_LEVEL		TYPEC_FSM_STATE				
R	R		R				

Address: STUSB_BLOCKBaseAddress + 0x11

Type: R

Reset: 0x01

Description: CC_STATUS register

[7]	**REVERSE**: Connection orientation, indicates CC pin used for PD communication 0: (STRAIGHT_CC1) 1: (TWISTED_CC2)
[6:5]	**SNK_POWER_LEVEL**: Note: This bit-field is valid only when POWER_MODE==POW_SNK 00: (CUR_DEFAULT) Rp standard current is connected 01: (CUR_1_5A) Rp 1.5A is connected 10: (CUR_3_0A) Rp 3.0A is connected 11: Reserved
[4:0]	**TYPEC_FSM_STATE**: Indicates Type-C FSM state 00000: (UNATTACHED_SNK) 00001: (ATTACHWAIT_SNK) 00010: (ATTACHED_SNK) 00011: (DEBUGACCESSORY_SNK) 00100: Reserved 00101: Reserved 00110: (SNK_2_SRC_PR_SWAP) Intermediate state during PR Swap from sink to source 00111: (TRYWAIT_SNK) 01000: (UNATTACHED_SRC) 01001: (ATTACHWAIT_SRC) 01010: (ATTACHED_SRC) 01011: (SRC_2_SNK_PR_SWAP) Intermediate state during PR Swap from source to sink

	01100: (TRY_SRC) 01101: (UNATTACHED_ACCESSORY) 01110: (ATTACHWAIT_ACCESSORY) 01111: (AUDIOACCESSORY) 10000: (UNORIENTEDDEBUGACCESSORY_SRC) 10001: (POWERED_ACCESSORY) 10010: (UNSUPPORTED_ACCESSORY) 10011: (TYPEC_ERRORRECOVERY) 10100: (TRYDEBOUNCE_SNK) Intermediate state towards TRY_SNK state 10101: (TRY_SNK) 10110: Reserved 10111: (TRYWAIT_SRC) 11000: (UNATTACHEDWAIT_SRC) VCONN intermediate discharge state 11001: (ORIENTEDDEBUGACCESSORY_SRC) 11010: (SRC_2_SNK_PR_SWAP_RD) Intermediate state during PR Swap from source to sink

CC_HW_FAULT_STATUS_0

CC_HW_FAULT_STATUS_0 register

7	6	5	4	3	2	1	0
TH_145_STATUS	RESERVED	VPU_OVP_FAULT_TRANS	VPU_VALID_TRANS	RESERVED	VCONN_SW_RVP_FAULT_TRANS	VCONN_SW_OCP_FAULT_TRANS	VCONN_SW_OVP_FAULT_TRANS
RC	R	RC	RC	R	RC	RC	RC

Address: STUSB_BLOCKBaseAddress + 0x12

Type: R

Reset: 0x10

Description: CC_HW_FAULT_STATUS_0 register

[7]	**TH_145_STATUS**: TBD
[5]	**VPU_OVP_FAULT_TRANS**: change in CS_OVP status
[4]	**VPU_VALID_TRANS**: change in VPUvalidity status
[2]	**VCONN_SW_RVP_FAULT_TRANS**: TBD
[1]	**VCONN_SW_OCP_FAULT_TRANS**: TBD
[0]	**VCONN_SW_OVP_FAULT_TRANS**: TBD

CC_HW_FAULT_STATUS_1

CC_HW_FAULT_STATUS_1 register

7	6	5	4	3	2	1	0
VPU_OVP_FAULT	VPU_VALID	VCONN_SW_RVP_FAULT_CC1	VCONN_SW_RVP_FAULT_CC2	VCONN_SW_OCP_FAULT_CC1	VCONN_SW_OCP_FAULT_CC2	VCONN_SW_OVP_FAULT_CC1	VCONN_SW_OVP_FAULT_CC2
R	R	R	R	R	R	R	R

Address: STUSB_BLOCKBaseAddress + 0x13

Type: R

Reset: 0x40

Description: CC_HW_FAULT_STATUS_1 register

[7]	**VPU_OVP_FAULT**
[6]	**VPU_VALID**
[5]	**VCONN_SW_RVP_FAULT_CC1**

[4]	**VCONN_SW_RVP_FAULT_CC2**
[3]	**VCONN_SW_OCP_FAULT_CC1**
[2]	**VCONN_SW_OCP_FAULT_CC2**
[1]	**VCONN_SW_OVP_FAULT_CC1**
[0]	**VCONN_SW_OVP_FAULT_CC2**

PRT_STATUS

PRT_STATUS register

7	6	5	4	3	2	1	0
PRL_TX_ERR	RESERVED	PRT_BIST_SENT	PRT_BIST_RECEIVED	PRL_MSG_SENT	PRL_MSG_RECEIVED	PRL_HW_RST_DONE	PRL_HW_RST_RECEIVED
RC	R	RC	RC	RC	RC	RC	RC

Address: STUSB_BLOCKBaseAddress + 0x16

Type: R

Reset: 0x00

Description: PRT_STATUS register

[7]	**PRL_TX_ERR**: 0: Cleared by I2C master 1: Interrupt for TX error on the Protocol Layer
[5]	**PRT_BIST_SENT**: TBD
[4]	**PRT_BIST_RECEIVED**: TBD
[3]	**PRL_MSG_SENT**: 0: Cleared by I2C master 1: Interrupt for message sent from the Protocol Layer when GoodCRC is received
[2]	**PRL_MSG_RECEIVED**: 0: Cleared by I2C master 1: Interrupt for Protocol Layer Message Received
[1]	**PRL_HW_RST_DONE**: 0: Cleared by I2C master 1: Interrupt for a PD hardware reset executed (hardware reset has to be completed to set the flag)
[0]	**PRL_HW_RST_RECEIVED**: 0: Cleared by I2C master 1: Interrupt for a PD hardware reset request coming from RX

PHY_STATUS

PHY_STATUS register

7	6	5	4	3	2	1	0
RX_MSG_STATUS			RESERVED	BUS_IDLE	TX_MSG_SUCC	TX_MSG_DISC	TX_MSG_FAIL
RC			R	RC	RC	RC	RC

Address: STUSB_BLOCKBaseAddress + 0x17

Type: R

Reset: 0x00

Description: PHY_STATUS register

[7:5]	**RX_MSG_STATUS**: TBD
[3]	**BUS_IDLE**: TBD

[2]	**TX_MSG_SUCC**: TBD
[1]	**TX_MSG_DISC**: TBD
[0]	**TX_MSG_FAIL**: TBD

PD_COMMAND

PD_COMMAND register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	PD_CMD					
R	R	R/W					

Address: STUSB_BLOCKBaseAddress + 0x1A

Type: R/W

Reset: 0x00

Description: PD_COMMAND register

[5:0]	**PD_CMD**: TBD

DEVICE_CTRL

DEVICE_CTRL register

7	6	5	4	3	2	1	0
PD_TOP_LAYER		PDO_READY	RDO_READY	VDM_READY	MSGID_CTRL	PHY_TX_RESET	RESERVED
R/W		W	R/W	R/W	R/W	W	R

Address: STUSB_BLOCKBaseAddress + 0x1D

Type: R/W

Reset: 0x20

Description: DEVICE_CTRL register

[7:6]	**PD_TOP_LAYER**: It is meaningful only is DEV_CUT[1:0] = TypeC + PD (STUSB46) 00: (PRL) PD top layer is hardware PRL (STUSB4620) 01: (PE) PD top layer is hardware PE (STUSB4610) Full SW control is needed 10: (DL) PD top layer is harware DPM (STUSB46 with Partial Auto-Run=1) SW control is needed 11: (SDL) PD top layer is harware DPM (STUSB46 withFull Auto-Run=1) Initialized by FTP_DEVICE_POWER_ROLE_CTRL[7:6]
[5]	**PDO_READY** Initialized by FTP_DEVICE_POWER_ROLE_CTRL[5]
[4]	**RDO_READY**: Initialized by FTP_DEVICE_POWER_ROLE_CTRL[4]
[3]	**VDM_READY**: Initialized by FTP_DEVICE_POWER_ROLE_CTRL[3]
[2]	**MSGID_CTRL**:
[1]	**PHY_TX_RESET**: 0: (NO_PHY_TX_RST) Do not reset transmitter of the physical layer 1: (PHY_TX_RST) Reset transmitter of the physical layer

ANALOG_CNTRL

ANALOG_CNTRL register

7	6	5	4	3	2	1	0
RESERVED				VCONN_ISEL_TH			
R				R/W			

Address: STUSB_BLOCKBaseAddress + 0x1E

Type: R/W

Reset: 0x0

Description: ANALOG_CNTRL register

[3:0]	**VCONN_ISEL_TH** Initialized by FTP_ANALOG_CNTRL[3:0]

MONITORING_CTRL_0

MONITORING_CTRL_0 register

7	6	5	4	3	2	1	0
VCONN_MONITOR	VCONN_UVLO_SEL	VBUS_RANGE_MONITORING_EN	VBUS_MONITORING_EN	RESERVED			
R/W	R/W	R	R	R			

Address: STUSB_BLOCKBaseAddress + 0x20

Type: R/W

Reset: 0xB0

Description: MONITORING_CTRL_0 register

[7]	**VCONN_MONITOR**: 0: (VCONN_MON_OFF) Off 1: (VCONN_MON_ON) Monitor On
[6]	**VCONN_UVLO_SEL**: 0: (UVLO_HIGH) Select high level UVLO threshold of 4.65 V 1: (UVLO_LOW) Select low level UVLO threshold of 2.65 V
[5]	**VBUS_RANGE_MONITORING_EN**: vbus monitoring
[4]	**VBUS_MONITORING_EN**: as soon as TypeC attached

MONITORING_CTRL_1

MONITORING_CTRL_1 register

7	6	5	4	3	2	1	0
VSEL_PDO							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x21

Type: R/W

Reset: 0x32

Description: MONITORING_CTRL_1 register

[7:0]	**VSEL_PDO**: monitor VBUS DAC VALUE

MONITORING_CTRL_2

MONITORING_CTRL_2 register

7	6	5	4	3	2	1	0
VSHIFT_HIGH				VSHIFT_LOW			
R/W				R/W			

Address: STUSB_BLOCKBaseAddress + 0x22

Type: R/W

Reset: 0xFF

Description: MONITORING_CTRL_2 register

[7:4]	**VSHIFT_HIGH**: shift register initialisation high level (set OVP level)
[3:0]	**VSHIFT_LOW**: shift register initialisation low level (set UVP level)

RESET_CTRL

RESET_CTRL register

7	6	5	4	3	2	1	0
RESERVED							RESET_SW_EN
R/W							R/W

Address: STUSB_BLOCKBaseAddress + 0x23

Type: R/W

Reset: 0x00

Description: RESET_CTRL register

[0]	**RESET_SW_EN**: Software reset 0: (SW_RESET_OFF) Software reset disabled 1: (SW_RESET_ON) Software reset enabled

POWER_ACCESSORY_CTRL

POWER_ACCESSORY_CTRL register

7	6	5	4	3	2	1	0
RESERVED					ALT_MOD_FAIL	NOT_POW_ACC	POW_ACC_SUP
R/W					R/W	R/W	R/W

Address: STUSB_BLOCKBaseAddress + 0x24

Type: R/W

Reset: 0x00

Description: POWER_ACCESSORY_CTRL register

[2]	**ALT_MOD_FAIL** 0: (ALT_MOD_ON) Alternate mode allowed 1: (ALT_MOD_FAIL) Alternate mode disabled – Used by Type-C FSM to go to UnSupported.Accessory
[1]	**NOT_POW_ACC** 0: (POW_ACC) Powered accessory present - Used by Type-C FSM to stay in Powered.Accessory state) 1: (NO_POW_ACC) Powered accessory not present – Used by Type-C FSM to go to Try.SNK state
[0]	**POW_ACC_SUP** 0: (POW_ACC_OFF) Powered accessory not supported - detection disabled in Type-C FSM 1: (POW_ACC_ON) Powered accessory supported - detection enabled in Type-C FSM

	Initialized by FTP_PORT_ROLE_CNTRL[5]

VBUS_DISCHARGE_TIME_CTRL

VBUS_DISCHARGE_TIME_CTRL register

7	6	5	4	3	2	1	0
DISCHARGE_TIME_TO_0V				DISCHARGE_TIME_TRANSITION			
R/W				R/W			

Address: STUSB_BLOCKBaseAddress + 0x25

Type: R/W

Reset: 0x0

Description: VBUS_DISCHARGE_TIME_CTRL register

[7:4]	**DISCHARGE_TIME_TO_0V**: Discharge time from any contract to OV 800 ms is the default in standard Initialized by FTP_DISCHARGE_TIME_CTRL[7:4]
[3:0]	**DISCHARGE_TIME_TRANSITION**: Discharge time from any contract to next one the default in standard is 270ms Initialized by FTP_DISCHARGE_TIME_CTRL[3:0]

VBUS_DISCHARGE_CTRL

VBUS_DISCHARGE_CTRL register

7	6	5	4	3	2	1	0
VBUS_DISCHARGE_EN	RESERVED						
R/W	R						

Address: STUSB_BLOCKBaseAddress + 0x26

Type: R/W

Reset: 0x00

Description: VBUS_DISCHARGE_CTRL register

[7]	**VBUS_DISCHARGE_EN**: TBD

VBUS_CTRL

VBUS_CTRL register

7	6	5	4	3	2	1	0
RESERVED						SINK_VBUS_EN	SOURCE_VBUS_EN
R						R/W	R/W

Address: STUSB_BLOCKBaseAddress + 0x27

Type: R/W

Reset: 0x00

Description: VBUS_CTRL register

[1]	**SINK_VBUS_EN** 0: (VBUS_EN_SNK_FORCE_DIS) Disable the forced VBUS_EN_SNK pin assertion 1: (VBUS_EN_SNK_FORCE) Force the VBUS EN SNK pin assertion

[0]	**SOURCE_VBUS_EN** 0: (VBUS_EN_SRC_FORCE_DIS) Disable the forced VBUS_EN_SRC pin assertion 1: (VBUS_EN_SRC_FORCE) Force the VBUS EN SRC pin assertion

POWER_ROLE_CTRL

POWER_ROLE_CTRL register

7	6	5	4	3	2	1	0
RERSERVED					POWER_ROLE		
R					R/W		

Address: STUSB_BLOCKBaseAddress + 0x28

Type: R/W

Reset: 0x0

Description: POWER_ROLE_CTRL register

[2:0]	**POWER_ROLE**: 000: (SRC) Source 001: (SNK_ACC) Sink with Accessory Support 010: (SNK) Snk without Accessory Support 011: (DRP) DRP 100: (DRP_TRY_SRC) DRP with Accessory and Try.SRC support 101: (DRP_TRY_SNK) DRP with Accessory and Try.SNK support Others: Do not use Initialized by FTP_DEVICE_POWER_ROLE_CTRL[2:0]

PE_FSM

PE_FSM register

7	6	5	4	3	2	1	0
PE_FSM_STATE							
R							

Address: STUSB_BLOCKBaseAddress + 0x29

Type: R

Reset: 0x00

Description: PE_FSM register

[7:0]	**PE_FSM_STATE**: Policy Engine Layer FSM state 000000: (PE_INIT) 000001: (PE_SOFT_RESET) 000010: (PE_HARD_RESET) 000011: (PE_SEND_SOFT_RESET) 000100: (PE_C_BIST) 000101: (PE_SRC_STARTUP) 000110: (PE_SRC_DISCOVERY) 000111: (PE_SRC_REQUEST_CAPABILITIES) 001000: (PE_SRC_SEND_CAPABILITIES) 001001: (PE_SRC_NEGOTIATE_CAPABILITIES) 001010: (PE_SRC_TRANSITION_SUPPLY) 001011: (PE_SRC_TSINK_TRANSACTION) 001100: (PE_SRC_TRANSITION_SUPPLY_2) 001101: (PE_SRC_DISABLED) 001110: (PE_SRC_READY) 001111: (PE_SRC_READY_SENDING) 010000: (PE_SRC_CAPABILITY_RESPONSE)

	010001: (PE_SNK_STARTUP) 010010: (PE_SNK_DISCOVERY) 010011: (PE_SNK_WAIT_FOR_CAPABILITIES) 010100: (PE_SNK_EVALUATE_CAPABILITIES) 010101: (PE_SNK_SELECT_CAPABILITIES) 010110: (PE_SNK_TRANSITION_SINK) 010111: (PE_SNK_READY) 011000: (PE_SNK_READY_SENDING) 011001: (PE_DB_CP_CHECK_FOR_VBUS) 011010: (PE_PRS_EVALUATE_PR_SWAP) 011011: (PE_PRS_SEND_PR_SWAP) 011100: (PE_PRS_ACCEPT_PR_SWAP) 011101: (PE_PRS_SRC_SNK_TRANSITION_TO_OFF_ST) 011110: (PE_PRS_SRC_SNK_TRANSITION_TO_OFF) 011111: (PE_PRS_SRC_SNK_SOURCE_OFF) 100000: (PE_PRS_SNK_SRC_TRANSITION_TO_OFF) 100001: (PE_PRS_SNK_SRC_SOURCE_ON) 100010: (PE_PRS_SNK_SRC_SOURCE_ON_2) 100011: (PE_PRS_ASSERT_RD) 100100: (PE_PRS_ASSERT_RP) 100101: (PE_DRS_EVALUATE_DR_SWAP) 100110: (PE_DRS_CHANGE_TO_DRP) 100111: (PE_DRS_REJECT_DR_SWAP) 101000: (PE_DRS_ACCEPT_DR_SWAP) 101001: (PE_DRS_WAIT_CHANGE) 101010: (PE_DRS_SEND_DR_SWAP) 101011: (PE_VCS_DFP_SEND_SWAP) 101100: (PE_VCS_DFP_SEND_SWAP2) 101101: (PE_VCS_DFP_SEND_SWAP3) 101110: (PE_VCS_DFP_WAIT_FOR_UFP_VCONN) 101111: (PE_VCS_DFP_TURN_ON_VCONN) 110000: (PE_VCS_DFP_TURN_OFF_VCONN) 110001: (PE_VCS_DFP_SEND_PS_RDY) 110010: (PE_VCS_UFP_REJECT_VCONN_SWAP) 110011: (PE_VCS_UFP_EVALUATE_SWAP) 110100: (PE_VCS_UFP_ACCEPT_SWAP) 110101: (PE_VCS_UFP_WAIT_FOR_DFP_VCONN) 110110: (PE_VCS_UFP_TURN_ON_VCONN) 110111: (PE_VCS_UFP_TURN_OFF_VCONN) 111000: (PE_VCS_UFP_SEND_PS_RDY) 111001: (PE_HARD_RESET_SHUTDOWN) 111010: (PE_HARD_RESET_RECOVERY) 111011: (PE_ATTENTION_RECEIVED) 111100: (PE_UFP_VDM_GET_VDM) 111101: (PE_UFP_VDM_SEND_VDM_ACK) 111110: (PE_UFP_VDM_SEND_VDM_NACK) 111111: (PE_ERRORRECOVERY)

SPARE_BITS

SPARE_BITS register

7	6	5	4	3	2	1	0

NC	VDD_OVLO_DISABLE	RESET_BY_LDO_DISABLE	VBUS_HIGH_LOW_BYPASS	VBUS_EN_SNK_INV	VSAFE0V_SEL	VBUS_EN_MASK_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: STUSB_BLOCKBaseAddress + 0x2E

Type: R/W

Reset: 0x00

Description: SPARE_BITS register

[7]	**NC** Initialized by FTP_SPARE[7]
[6]	**VDD_OVLO_DISABLE** Initialized by FTP_SPARE[6]
[5]	**RESET_BY_LDO_DISABLE** 0: (RST_BY_LDO_ON) Enable device reset by forcing VREG_1V2 to 1.8V or higher 1: (RST_BY_LDO_OFF) Disable device reset by forcing VREG_1V2 to 1.8V or higher Initialized by FTP_SPARE[5]
[4]	**VBUS_HIGH_LOW_BYPASS** Initialized by FTP_SPARE[4]
[3]	**VBUS_EN_SNK_INV** 0: (VBUS_EN_SNK_NOT_INV) VBUS_EN_SNK not inverted 1: (VBUS_EN_SNK_INV) VBUS_EN_SNK output inverted Initialized by FTP_SPARE[3]
[2:1]	**VSAFE0V_SEL** 00: (VSAFE0V_0_6) vsafe0V threshold=0.6V 01: (VSAFE0V_0_9) vsafe0V threshold=0.9V 10: (VSAFE0V_1_2) vsafe0V threshold=1.2V 11: (VSAFE0V_1_8) vsafe0V threshold=1.8V Initialized by FTP_SPARE[2:1]
[0]	**VBUS_EN_MASK_DIS** Initialized by FTP_SPARE[0]

DEVICE_ID

DEVICE_ID register

7	6	5	4	3	2	1	0
VB47_NOT_VB39	RESERVED		ID			DEV_CUT	
R	R		R			R	

Address: STUSB_BLOCKBaseAddress + 0x2F

Type: R

Reset: 0x90

Description: DEVICE_ID register

[7]	**VB47_NOT_VB39:** (Static, hardwired in analog part) 1: VB47 device 0: VB39 device Note: For verification purpose the reset value must be 1.
[4:2]	**ID**: 010: for Cut2.0 011: for Cut2.1 100: for Cut2.2
[1:0]	**DEV_CUT**: Initialized by FTP_DEVICE_CUT[7:6]

RX_HEADER_LOW

RX_HEADER_LOW register

7	6	5	4	3	2	1	0
RX_HEADER_7_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x31

Type: R

Reset: 0x00

Description: RX_HEADER_LOW register

[7:0]	**RX_HEADER_7_0**: TBD

RX_HEADER_HIGH

RX_HEADER_HIGH register

7	6	5	4	3	2	1	0
RX_HEADER_15_8							
R							

Address: STUSB_BLOCKBaseAddress + 0x32

Type: R

Reset: 0x00

Description: RX_HEADER_HIGH register

[7:0]	**RX_HEADER_15_8**: TBD

RX_DATA_OBJ1_0

RX_DATA_OBJ1_0 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ1_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x33

Type: R

Reset: 0x00

Description: RX_DATA_OBJ1_0 register

[7:0]	**RX_DATA_OBJ1_0**

RX_DATA_OBJ1_1

RX_DATA_OBJ1_1 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ1_1							
R							

Address: STUSB_BLOCKBaseAddress + 0x34

Type: R

Reset: 0x00

Description: RX_DATA_OBJ1_1 register

[7:0]	**RX_DATA_OBJ1_1**

RX_DATA_OBJ1_2

RX_DATA_OBJ1_2 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ1_2							
R							

Address: STUSB_BLOCKBaseAddress + 0x35

Type: R

Reset: 0x00

Description: RX_DATA_OBJ1_2 register

[7:0]	**RX_DATA_OBJ1_2**

RX_DATA_OBJ1_3

RX_DATA_OBJ1_3 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ1_3							
R							

Address: STUSB_BLOCKBaseAddress + 0x36

Type: R

Reset: 0x00

Description: RX_DATA_OBJ1_3 register

[7:0]	**RX_DATA_OBJ1_3**

RX_DATA_OBJ2_0

RX_DATA_OBJ2_0 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ2_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x37

Type: R

Reset: 0x00

Description: RX_DATA_OBJ2_0 register

[7:0]	**RX_DATA_OBJ2_0**

RX_DATA_OBJ2_1

RX_DATA_OBJ2_1 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ2_1							
R							

Address: STUSB_BLOCKBaseAddress + 0x38

Type: R

Reset: 0x00

Description: RX_DATA_OBJ2_1 register

[7:0]	**RX_DATA_OBJ2_1**

RX_DATA_OBJ2_2

RX_DATA_OBJ2_2 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ2_2							
R							

Address: STUSB_BLOCKBaseAddress + 0x39

Type: R

Reset: 0x00

Description: RX_DATA_OBJ2_2 register

[7:0]	**RX_DATA_OBJ2_2**

RX_DATA_OBJ2_3

RX_DATA_OBJ2_3 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ2_3							
R							

Address: STUSB_BLOCKBaseAddress + 0x3A

Type: R

Reset: 0x00

Description: RX_DATA_OBJ2_3 register

[7:0]	**RX_DATA_OBJ2_3**

RX_DATA_OBJ3_0

RX_DATA_OBJ3_0 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ3_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x3B

Type: R

Reset: 0x00

Description: RX_DATA_OBJ3_0 register

[7:0]	**RX_DATA_OBJ3_0**

RX_DATA_OBJ3_1

RX_DATA_OBJ3_1 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ3_1							
R							

Address: STUSB_BLOCKBaseAddress + 0x3C

Type: R

Reset: 0x00

Description: RX_DATA_OBJ3_1 register

[7:0]	**RX_DATA_OBJ3_1**

RX_DATA_OBJ3_2

RX_DATA_OBJ3_2 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ3_2							
R							

Address: STUSB_BLOCKBaseAddress + 0x3D

Type: R

Reset: 0x00

Description: RX_DATA_OBJ3_2 register

[7:0]	**RX_DATA_OBJ3_2**

RX_DATA_OBJ3_3

RX_DATA_OBJ3_3 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ3_3							
R							

Address: STUSB_BLOCKBaseAddress + 0x3E

Type: R

Reset: 0x00

Description: RX_DATA_OBJ3_3 register

[7:0]	**RX_DATA_OBJ3_3**

RX_DATA_OBJ4_0

RX_DATA_OBJ4_0 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ4_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x3F

Type: R

Reset: 0x00

Description: RX_DATA_OBJ4_0 register

[7:0]	**RX_DATA_OBJ4_0**

RX_DATA_OBJ4_1

RX_DATA_OBJ4_1 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ4_1							
R							

Address: STUSB_BLOCKBaseAddress + 0x40

Type: R

Reset: 0x00

Description: RX_DATA_OBJ4_1 register

[7:0]	**RX_DATA_OBJ4_1**

RX_DATA_OBJ4_2

RX_DATA_OBJ4_2 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ4_2							
R							

Address: STUSB_BLOCKBaseAddress + 0x41

Type: R

Reset: 0x00

Description: RX_DATA_OBJ4_2 register

[7:0]	**RX_DATA_OBJ4_2**

RX_DATA_OBJ4_3

RX_DATA_OBJ4_3 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ4_3							
R							

Address: STUSB_BLOCKBaseAddress + 0x42

Type: R

Reset: 0x00

Description: RX_DATA_OBJ4_3 register

[7:0]	**RX_DATA_OBJ4_3**

RX_DATA_OBJ5_0

RX_DATA_OBJ5_0 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ5_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x43

Type: R

Reset: 0x00

Description: RX_DATA_OBJ5_0 register

[7:0]	**RX_DATA_OBJ5_0**

RX_DATA_OBJ5_1

RX_DATA_OBJ5_1 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ5_1							
R							

Address: STUSB_BLOCKBaseAddress + 0x44

Type: R

Reset: 0x00

Description: RX_DATA_OBJ5_1 register

[7:0]	**RX_DATA_OBJ5_1**

RX_DATA_OBJ5_2

RX_DATA_OBJ5_2 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ5_2							
R							

Address: STUSB_BLOCKBaseAddress + 0x45

Type: R

Reset: 0x00

Description: RX_DATA_OBJ5_2 register

[7:0]	**RX_DATA_OBJ5_2**

RX_DATA_OBJ5_3

RX_DATA_OBJ5_3 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ5_3							
R							

Address: STUSB_BLOCKBaseAddress + 0x46

Type: R

Reset: 0x00

Description: RX_DATA_OBJ5_3 register

[7:0]	**RX_DATA_OBJ5_3**

RX_DATA_OBJ6_0

RX_DATA_OBJ6_0 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ6_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x47

Type: R

Reset: 0x00

Description: RX_DATA_OBJ6_0 register

[7:0]	**RX_DATA_OBJ6_0**

RX_DATA_OBJ6_1

RX_DATA_OBJ6_1 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ6_1							
R							

Address: STUSB_BLOCKBaseAddress + 0x48

Type: R

Reset: 0x00

Description: RX_DATA_OBJ6_1 register

[7:0]	**RX_DATA_OBJ6_1**

RX_DATA_OBJ6_2

RX_DATA_OBJ6_2 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ6_2							
R							

Address: STUSB_BLOCKBaseAddress + 0x49

Type: R

Reset: 0x00

Description: RX_DATA_OBJ6_2 register

[7:0]	**RX_DATA_OBJ6_2**

RX_DATA_OBJ6_3

RX_DATA_OBJ6_3 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ6_3							
R							

Address: STUSB_BLOCKBaseAddress + 0x4A

Type: R

Reset: 0x00

Description: RX_DATA_OBJ6_3 register

[7:0]	**RX_DATA_OBJ6_3**

RX_DATA_OBJ7_0

RX_DATA_OBJ7_0 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ7_0							
R							

Address: STUSB_BLOCKBaseAddress + 0x4B

Type: R

Reset: 0x00

Description: RX_DATA_OBJ7_0 register

[7:0]	**RX_DATA_OBJ7_0**

RX_DATA_OBJ7_1

RX_DATA_OBJ7_1 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ7_1							
R							

Address: STUSB_BLOCKBaseAddress + 0x4C

Type: R

Reset: 0x00

Description: RX_DATA_OBJ7_1 register

[7:0]	**RX_DATA_OBJ7_1**

RX_DATA_OBJ7_2

RX_DATA_OBJ7_2 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ7_2							
R							

Address: STUSB_BLOCKBaseAddress + 0x4D

Type: R

Reset: 0x00

Description: RX_DATA_OBJ7_2 register

[7:0]	**RX_DATA_OBJ7_2**

RX_DATA_OBJ7_3

RX_DATA_OBJ7_3 register

7	6	5	4	3	2	1	0
RX_DATA_OBJ7_3							
R							

Address: STUSB_BLOCKBaseAddress + 0x4E

Type: R

Reset: 0x00

Description: RX_DATA_OBJ7_3 register

[7:0]	**RX_DATA_OBJ7_3**

DPM_PDO_NUMB

DPM_PDO_NUMB register

7	6	5	4	3	2	1	0
DPM_SRC_PDO_NUMB			RESERVED		DPM_SNK_PDO_NUMB		
R/W			R		R/W		

Address: STUSB_BLOCKBaseAddress + 0x70

Type: R/W

Reset: 0x0

Description: DPM_PDO_NUMB register

[7:5]	**DPM_SRC_PDO_NUMB**: Initialized by SRC_PDO_FILL_0[7:6] + 0x2
[2:0]	**DPM_SNK_PDO_NUMB**: Initialized by SNK_PDO_FILL_0[6] + 0x2

DPM_SRC_PDO1_0

DPM_SRC_PDO1_0 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO1_0							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x71

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO1_0 register

[7:0]	**DPM_SRC_PDO1_0**

DPM_SRC_PDO1_1

DPM_SRC_PDO1_1 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO1_1							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x72

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO1_1 register

[7:0]	**DPM_SRC_PDO1_1**

DPM_SRC_PDO1_2

DPM_SRC_PDO1_2 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO1_2							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x73

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO1_2 register

[7:0]	**DPM_SRC_PDO1_2**: Initialized to 0b00xx0001 with xx = SRC_PDO_FILL_0[1:0]

DPM_SRC_PDO1_3

DPM_SRC_PDO1_3 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO1_3							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x74

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO1_3 register

[7:0]	**DPM_SRC_PDO1_3**: Initialized to 0x08

DPM_SRC_PDO2_0

DPM_SRC_PDO2_0 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO2_0							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x75

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO2_0 register

[7:0]	**DPM_SRC_PDO2_0**

DPM_SRC_PDO2_1

DPM_SRC_PDO2_1 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO2_1							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x76

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO2_1 register

[7:0]	**DPM_SRC_PDO2_1**

DPM_SRC_PDO2_2

DPM_SRC_PDO2_2 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO2_2							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x77

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO2_2 register

[7:0]	**DPM_SRC_PDO2_2**

DPM_SRC_PDO2_3

DPM_SRC_PDO2_3 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO2_3							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x78

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO2_3 register

[7:0]	**DPM_SRC_PDO2_3**

DPM_SRC_PDO3_0

DPM_SRC_PDO3_0 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO3_0							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x79

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO3_0 register

[7:0]	**DPM_SRC_PDO3_0**

DPM_SRC_PDO3_1

DPM_SRC_PDO3_1 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO3_1							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x7A

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO3_1 register

[7:0]	**DPM_SRC_PDO3_1**

DPM_SRC_PDO3_2

DPM_SRC_PDO3_2 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO3_2							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x7B

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO3_2 register

[7:0]	**DPM_SRC_PDO3_2**

DPM_SRC_PDO3_3

DPM_SRC_PDO3_3 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO3_3							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x7C

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO3_3 register

[7:0]	**DPM_SRC_PDO3_3**

DPM_SRC_PDO4_0

DPM_SRC_PDO4_0 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO4_0							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x7D

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO4_0 register

[7:0]	**DPM_SRC_PDO4_0**

DPM_SRC_PDO4_1

DPM_SRC_PDO4_1 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO4_1							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x7E

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO4_1 register

[7:0]	**DPM_SRC_PDO4_1**

DPM_SRC_PDO4_2

DPM_SRC_PDO4_2 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO4_2							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x7F

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO4_2 register

[7:0]	**DPM_SRC_PDO4_2**

DPM_SRC_PDO4_3

DPM_SRC_PDO4_3 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO4_3							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x80

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO4_3 register

[7:0]	**DPM_SRC_PDO4_3**

DPM_SRC_PDO5_0

DPM_SRC_PDO5_0 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO5_0							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x81

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO5_0 register

[7:0]	**DPM_SRC_PDO5_0**

DPM_SRC_PDO5_1

DPM_SRC_PDO5_1 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO5_1							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x82

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO5_1 register

[7:0]	**DPM_SRC_PDO5_1**

DPM_SRC_PDO5_2

DPM_SRC_PDO5_2 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO5_2							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x83

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO5_2 register

[7:0]	**DPM_SRC_PDO5_2**

DPM_SRC_PDO5_3

DPM_SRC_PDO5_3 register

7	6	5	4	3	2	1	0
DPM_SRC_PDO5_3							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x84

Type: R/W

Reset: 0x00

Description: DPM_SRC_PDO5_3 register

[7:0]	**DPM_SRC_PDO5_3**

DPM_REQ_RDO3_0

DPM_REQ_RDO3_0 register

7	6	5	4	3	2	1	0
DPM_REQ_RDO3_0							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x91

Type: R/W

Reset: 0x00

Description: DPM_REQ_RDO3_0 register

[7:0]	**DPM_REQ_RDO3_0**

DPM_REQ_RDO3_1

DPM_REQ_RDO3_1 register

7	6	5	4	3	2	1	0
DPM_REQ_RDO3_1							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x92

Type: R/W

Reset: 0x00

Description: DPM_REQ_RDO3_1 register

[7:0]	**DPM_REQ_RDO3_1**

DPM_REQ_RDO3_2

DPM_REQ_RDO3_2 register

7	6	5	4	3	2	1	0
DPM_REQ_RDO3_2							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x93

Type: R/W

Reset: 0x00

Description: DPM_REQ_RDO3_2 register

[7:0]	**DPM_REQ_RDO3_2**

DPM_REQ_RDO3_3

DPM_REQ_RDO3_3 register

7	6	5	4	3	2	1	0
DPM_REQ_RDO3_3							
R/W							

Address: STUSB_BLOCKBaseAddress + 0x94

Type: R/W

Reset: 0x00

Description: DPM_REQ_RDO3_3 register

[7:0]	**DPM_REQ_RDO3_3**