

Hello, I would like to know what is wrong with my current configuration of SPI module. I can see data in the TX FIFO, but its not getting transmitted.

I am using the SPC570S40E1 microcontroller.

SPI Port Configuration

```
void Initialize_SPI_Port(void)
{
// Using DSPI 0

    // DSPI0_CS -- PA[0] , Pin #2, PAD[0]
    STUH2_MSCR_TOTL_B_SSS = PAI_SPC5_SSS(1)
```

```
// DSPI0_SCK -- PA[3] , Pin #3, PAD[3]
SIUL2.MSCR_IO[3].B.SSS = PAL_SPC5_SSS(1);
```

```
// DSPI0_MISO -- PA[4], Pin #4, PAD[4]
SIUL2.MSCR_IO[4].B.IBE = 1;
SIUL2.MSCR_MUX[624-512].R = PA1_SPC5_SSS(1)
```

```
// DSPI0_MOSI -- PA[7], Pin #5, PAD[7]
SIUL2.MSCR_IO[7].B.SSS = PAL_SPC5_SSS(1);
```

```
}
```

SPI Module configuration

```
void Initialize_DSPI0(void)
```

```

// Configure DSPI0 Module Configuration Register ( DSPI0_MCR )
// MSTR           - 0      , Master mode
// CONT_SCKE     - 0      , Continuous SCK disabled
// DCONF          - 00    , SPI
// FRZ            - 0      , Do not halt serial transfers in debug mode
// MTFE           - 0      , Modified Timing Format disabled
// ROOE           - 0      , (Receive FIFO Overflow Overwrite) Incoming data is ignored
// PCSIS0         - 1      , Inactive state of PCS0 is high
// MDIS           - 1      , Allow external logic to disable DSPI clocks
// DIS_TXF        - 0      , TX FIFO enabled
// DIS_RXF        - 0      , RX FIFO enabled
// XSPI           - 0      , Normal SPI Mode
// FCPPCS         - 1      , Fast Continuous PCS mode.
// PES            - 0      , SPI frame transmission continues
// HALT           - 0      , Start transfers
DSPI_0.MCR.R = 0x10004;

// Configure CTAR0 and CTAR1 ( Clock and Transfer Attributes ) Register
// Two transfer attributes used. CTAR0 configured for 16-bit frame size. CTAR1 configured for 8-bit frame size.
// DBR             - 0      , Baud rate not doubled
// FMSZ(for CTAR0) - 1111 , Frame size set to FMSZ + 1 or 16 bits
// CPOL            - 0      , Clock Polarity - Inactive state value of SCK is low
// CPHA            - 0      , Data is captured on the leading edge of SCK and changed on the following edge
// LSBFE           - 0      , MSB is transferred first
// PCSSCK          - 00    , PCS to SCK Prescaler value is 1
// PASC            - 00    , Sets the delay between last SCK edge to negation of CS, 00 sets the Prescaler value to 1
// PDT             - 00    , Sets the delay between negation of PCS at end of frame to assertion beginning of next frame, 00 - Presc
// PBR             - 00    , Baud Rate Prescaler, set to 2. Available values - 2,3,5, and 7
// CSSCK           - 0000 , PCS to SCK Delay Scaler set to 2
// ASC             - 0000 , Scaler value for the After SCK Delay, set to 2
// DT              - 0000 , Scaler value set to 2
// BR              - 0011 , Baud Rate scaler set to 8

/* ----- Calculation -----
   SPI Baud Rate      = (Fp / PBR) * ( [1 + DBR]/BR ) , Fp = Peripheral Clock / AC0_DC3 = 64/1 = 64Mhz
                           = (64/2)           * ([1]/8 )
                           = 64/16
                           = 4Mhz
*/
DSPI_0.CTAR[0].R = 0x78000003;
DSPI_0.CTAR[1].R = 0x38000003;

```

SR	42013000	TCF TFUF CMDTCF TFIWF TXCTR RXCTR	Not complete No underflow Not completed Valid 3 0	TXRXS TFFF SPEF RFDF TXNXTPTR POPNXTPTR	Enabled Not full No error Empty 0 0	EOQF 8SYF RFOF CMDFFF	No Not busy No overflow Not full
RSER	00000000	TCF_RE TFUF_RE CMDTCF_RE TFIWF_RE CMDFFF_OIRS	Disabled Disabled Disabled Disabled Interrupt	CMDFFF_RE TFFF_RE SPEF_RE RFDF_RE	Disabled Disabled Disabled Disabled	EOQF_RE TFFF_DIRS RFOF_RE RFDF_DIRS	Disabled Disabled Disabled Interrupt
PUSHHR	0000000A	TXDATA	000A				

POPR	XXXXXXXX	<u>DATA_IN</u>					
TXFR0	04010005	TXCMD_TXDATA	0401	TXDATA	0005		
TXFR1	00010005	TXCMD_TXDATA	0001	TXDATA	0005		
TXFR2	1801000A	TXCMD_TXDATA	1801	TXDATA	000A		
TXFR3	00000000	TXCMD_TXDATA	0000	TXDATA	0000		
RXFR0	00000000						
RXFR1	00000000						
RXFR2	00000000						
RXFR3	00000000						

SREX 00000030 CMDCTR 3 CMDNXTPTR 0